TECHNICAL BULLETIN

DIAGNOSTIC PROGRAMS

FOR

AUTOMATIC

TELEPHONE

CENTRAL OFFICE

AN/TTC-38(V)

HEADQUARTERS, DEPARTMENT OF THE ARMY

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TECHNICAL BULLETIN

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Purpose and Scope. *a.* The diagnostic programs for Automatic Telephone Central Office AN/TTC-38(V) are essentially off-line functional fault detection programs. A particular order of program unit usage is a typical expectation in any diagnostic program package; however, each diagnostic program for the AN/TTC-38(V) is considered a separate entity and therefore, the program units can be executed in any order.

b. The diagnostic package contains two basic types of tests. One uses manual execution of instructions and control of the logic for detection purposes and the other depends upon program control and analysis of the resultant data flow. Detailed test/programs exercise instruction sequences and data flow to isolate failures to the functional level defined by each test. The level of function fault detection varies with the detectability of unique failure characteristics for the different units.

c. The introduction of various manual instruction and display activities from the Maintenance Control Panel establishes the basic "sanity" of the communication system, provides for the keying-in of a basic loader program, and confirms the capability of input operation and the continuation to storage and retrieval of data for error-free performance.

d. To assist in fault isolation, data flow diagrams have been provided, where possible, to show a pictorial order of program execution, the possible program halts to be encountered, and the particular problems signified by the program halt. The program halts designated on the flow diagrams represent points in the diagnostic program where technical assistance personnel must make a decision.

EXHIBIT A

MAINTENANCE CONTROL PANEL DIAGNOSTIC PROGRAM

Section I. GENERAL

There are two individual sections of the Maintenance Control Panel diagnostic program: manual and programmed tests. The two test sections are independent and therefore provide verification of the logic, associated with the Maintenance Control Panel, from different vantage points. Both the manual and the programmed diagnostic programs are generally redundant in their ability to check the Maintenance Control Panel controls and indicators. Therefore, the programmed test for this purpose would normally be used since it is quicker. However, if problems exist, whereby the program cannot be loaded into memory, the manual diagnostic program can be used.

Section II. MANUAL DIAGNOSTIC PROGRAM

THE FOLLOWING PROCEDURES ARE USED FOR INITIAL CONDITIONING

- 1. Set the MEMORY guarded switch to the UNPROTECTED position.
- 2. Set the PARITY ERROR HALT toggle switch to OFF.
- 3. Set the CLOCK OPERATE CONTROL rotary switch to CONT.
- 4. Set the ADV-RPT toggle switch to ADV.
- 5. Set the REAL TIME CLOCK guarded switch to the DISABLE position.
- 6. Set the RUN/ONE INSTR toggle switch to RUN.
- 7. Set the system status panel CONTROL TRANSFER guarded switch to DISABLE and observe that:
 - a. PROCESSOR STATUS OFF-LINE Indicator is illuminated.
 - b. ACTIVE indicator is illuminated.
 - c. PRGM HALT indicator is illuminated.
- 8. Press the NORMAL HALT pushbutton switch and observe that:
 - a. PRGM HALT indicator extinguishes.
 - b. PRCS HALT indicator illuminates.
 - c. ACTIVE indicator extinguishes.
- 9. Press and hold the LAMP TEST pushbutton switch.
- 10. Observe that all Maintenance Control Panel indicators, except the other PRCS IDENT indicator, illuminate.
- 11. Release the LAMP TEST pushbutton switch and observe that all indicators illuminated in step 10 above are extinguished.

THE FOLLOWING PROCEDURES TEST THE CLOCK OPERATE CONTROL FUNCTIONS

- 12 Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the CLOCK OPERATE CONTROL to SINGLE PULSE.
- 13. Set the ADV-RPT toggle switch to RPT and observe that either the P1, P2, or P3 indicator lamp is illuminated.
- 14. Press the INITIATE pushbutton switch and observe that the same indicator lamp observed in step 13 above is still illuminated.
- 15. Set the ADV-RPT toggle switch to ADV.
- 16. Press the INITIATE pushbutton switch and observe that the next higher numbered indicator lamp illuminates. For example, if the P3 indicator lamp was illuminated in step 14 above, the P1 indicator lamp should now illuminate.

- 17. Set the ADV-RPT toggle switch to RPT.
- 18. Press the INITIATE pushbutton switch and observe that the same indicator lamp Illuminated in step 16 above remains illuminated.
- 19. Set the ADV-RPT toggle switch to ADV.
- 20. Press the INITIATE pushbutton switch and observe that the next higher numbered indicator lamp illuminates.
- 21. Set the ADV-RPT toggle switch to RPT.
- 22. Press the INITIATE pushbutton switch and observe that the same indicator lamp illuminated in step 20 above remains illuminated.
- 23. Set the CLOCK OPERATE CONTROL rotary switch to CONT and observe that the P1, P2, and P3 indicator lamps extinguish.
- 24. Set the ADV-RPT toggle switch to ADV.

THE FOLLOWING PROCEDURES TEST THE MEMORY STORE AND DISPLAY FUNCTIONS

- 25. Set the REGISTER SELECT rotary switch to MEM.
- 26. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 27. Set the ASR toggle switches to 010000.
- 28. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays the contents of memory address 10000. If the memory was cleared before performing this step, the BUS INDICATOR will display all 0's.
- 29. Set the REGISTER SELECT rotary switch to EOA and observe that the BUS INDICATOR displays a reading of 00010000.

NOTE

This is the effective operand address which was entered into memory in steps 27 and 28 above.

- 30. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to MEM.
- 31. Set the WSR toggle switches to all 7's.
- 32. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 77777777.
- 33. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 34. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays all 7's.

NOTE

This is the new contents of memory address 010000.

THE FOLLOWING PROCEDURES TEST THE SEQUENTIAL STORE FUNCTIONS

- 35. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 36. Set the WSR and the ASR toggle switches to all o's.
- 37. Set the RUN//ONE INSTR toggle switch to RUN.
- 38. Press the INITIATE pushbutton switch.
- 39. Set the OPERATIONAL CONTROL rotary switch to STORE SEQL and the REGISTER SELECT to MEM.
- 40. Observe that the BUS INDICATOR displays a reading of 77777777.
- 41. Set the WSR toggle switches to all 7's.
- 42. Press and hold the COORDINATE pushbutton switch and then press the INITIATE pushbutton switch.
- 43. Observe that the PRCS HALT indicator extinguishes and the ACTIVE indicator illuminates.

NOTE

The above procedures causes 77777777 to be stored in all memory addresses from the address set in step 36 above (memory page 0, address 0).

- 44. Press the NORMAL HALT pushbutton switch and observe that:
 - a. PRCS HALT indicator illuminates.
 - b. ACTIVE indicator extinguishes.
 - c. BUS INDICATOR displays a reading of 77777777.
- 45. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 46. Set the ASR toggle switches to 051000.
- 47. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 48. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays all 7's.

NOTE

Contents of memory page 0, location 11000.

- 49. Set the ASR toggle switches to 15000.
- 50. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 77777777.

NOTE

Contents of memory page 1, location 11000.

- 51. Set the ASR toggle switches to 251000.
- 52. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 77777777.

NOTE

Contents of memory page 2, location 11000.

THE FOLLOWING PROCEDURES TEST THE WORD SWITCH REGISTER FUNCTIONS

- 53. Set the WSR toggle switches to 01234567.
- 54. Set the ASR toggle switches to 037774.
- 55. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 01234567.
- 56. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 57. Set the WSR toggle switches to all 0's.
- 58. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00000000.
- 59. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 60. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays all 0's.

THE FOLLOWING PROCEDURES TEST THE REGISTER SELECTION FUNCTION

- 61. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 62. Set the WSR toggle switches to all 7's.
- 63. Set the REGISTER SELECT rotary switch, in sequence, to each position listed on the attached Table X. Press the INITIATE pushbutton switch after each setting and observe that the BUS INDICATOR displays the numerical value listed.

-	Table X
REGISTER SELECT	BUS INDICATOR
rotary switch	reading
SBR	00177777
LSR	01000077
OAR	03707777
IAR	03707777
MO	XXXXXXXX
MEM	7777777
PEX	00377777
PC	00077777
EOA	00077777
A	7777777
В	7777777
Q	7777777
IR	7777777
CPS	3777020x (NOTE)
CPD	77770200
BR	00000770
SHC	0000000
RTC	1777777
SC1	00000X00
SC2	XXXXXXXX

NOTE

DATA WORD and INSTR WORD indicators illuminate. WSR bit 21 should equal 0. Observe and record the indications of WSR bits 22 and 23 for later checks outlined in Section V.

THE FOLLOWING PROCEDURES TEST THE REGISTER CLEARING FUNCTIONS

- 64. Set the REGISTER SELECT rotary switch to PEX.
- 65. Press the CLEAR pushbutton switch and observe that:
 - a. DATA WORD indicator extinguishes.
 - b. INSTR WORD indicator extinguishes.
 - c. BUS INDICATOR displays a reading of 00000000.
- 65.1. Set the WSR and ASR toggle switches to all 0's.
- 66. Set the REGISTER SELECT rotary switch, in sequence, to each position listed on the attached Table XX and observe that the BUS INDICATOR displays the numerical value listed.

	Table XX
REGISTER SELECT	BUS INDICATOR
rotary switch	reading
SBR	0000000
LSR	0000000
OAR	00100000
IAR	00100000
MO	7777777
MEM	0000000
PEX	0000000
PC	0000000
EOA	0000000
A	0000000
В	0000000
Q	0000000
IR	0000000
CPS	0010000X (NOTE)
CPD	4000000
BR	0000000
SHC	0000000
RTC	0000000
SC1	0000000
SC2	0000000

NOTE

WSR bit 21 should equal 0. Observe and record the indications of WSR bits 22 and 23 for later checks outlined in Section V.

THE FOLLOWING PROCEDURES TEST THE CONTROL PANEL INSTRUCTIONS FUNCTIONS

- 67. Press the CLEAR pushbutton switch.
- 68. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR.
- 69. Set the WSR toggle switches to 12200001. This number represents an instruction (ADDC 1) which added 1 to the content of the accumulator (A register).
- 70. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays all 0's.
- 71. Set the REGISTER SELECT rotary switch to IR and observe that the BUS INDICATOR displays a reading of 12200001.
- 72. Set the REGISTER SELECT rotary switch to position A and observe that the BUS INDICATOR displays a reading of 00000001.
- 73. Set the RUN/ONE INSTR toggle switch to RUN.
- 74. Press the INITIATE pushbuilton switch and observe that the PRCS HALT indicator extinguishes and the ACTIVE indicator illuminates.
- 75. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates and the ACTIVE indicator extinguishes.
- 76. Observe that the BUS INDICATOR displays any number except 00000001.

NOTE

While the ACTIVE Indicator was illuminated, the processor repeatedly executed the ADDC 1 instruction; the number one was added to the accumulator many times. The number displayed in step 76 above is the sum of this repetitive addition process. If a BUS INDICATOR reading of 00000001 is displayed, repeat the procedure at least once to verify that there is a malfunction.

THE FOLLOWING PROCEDURES TEST THE ONE-INSTRUCTION FUNCTION

- 77. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 78. Set the WSR toggle switches to all 7's.
- 79. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 80. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 77777777.
- 81. Set the REGISTER SELECT rotary switch to PEX.
- 82. Set the WSR toggle switches to 00050000.
- 83. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00050000.
- 84. Set the REGISTER SELECT rotary switch to MEM.
- 85. Set the OPERATIONAL CONTROL rotary switch to STORE SEQL.
- 86. Set the WSR toggle switches to 55037774.
- 87. Set the ASR toggle switches to 00050000.
- 88. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 55037774.
- 89. Set the WSR toggle switches to all 0's.
- 90. Set the REGISTER SELECT rotary switch to position A and the OPERATIONAL CONTROL to CMPT.
- 91. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 77777777.

THE FOLLOWING PROCEDURES TEST THE FUNCTION CODE AND ADDRESS SWITCH REGISTER FUNCTION

- 92. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INST.
- 93. Set the WSR toggle switches to 55037756.
- 94. Set the function code to 77.
- 95. Set the ASR toggle switches to 377777.

- 96. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 77377777.
- 97. Set the function code to 00.
- 98. Set the ASR toggle switches to 00000.
- 99. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays all 0's.

THE FOLLOWING PROCEDURES TEST THE REAL TIME CLOCK FUNCTION

- Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 101. Set the WSR toggle switches to 00044777 (memory page 0, location 044777).
- 102. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00044777.
- Set the OPERATIONAL CONTROL rotary switch to STORE SEQL and the REGISTER SELECT to MEM.
- 104. Set the WSR toggle switch to the settings shown in a through d below, in sequence, and press the INITIATE pushbutton switch after each setting. Observe that the BUS INDICATOR displays the indicated instruction word.
 - 00160000. a.
 - b. 55230707.
 - 60144777. C. 22045000.
 - d.
- Verify that the REAL TIME CLOCK guarded switch is in the DISABLE position. 105.
- Set the REGISTER SELECT rotary switch to RTC and observe that the BUS INDICATOR displays all 0's. 106.
- 107. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 108. Set the WSR togale switches to 00045000.
- Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00045000. 109.
- 110 Set the OPERATIONAL CONTROL rotary switch to CMPT.
- Set the RUN/ONE INSTR toggle switch to RUN. 111.
- 112. Press the INITIATE pushbutton switch and observe that the PRGM HALT indicator extinguishes and the ACTIVE indicator illuminates.
- Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates and the ACTIVE 113. indicator extinguishes.
- 114. Set the REGISTER SELECT rotary switch to RTC and observe that the BUS INDICATOR displays all 0's.
- Set the REAL TIME CLOCK guarded switch to the ENABLE position. 115.
- 116. Press the INITIATE pushbutton switch and observe that the PRCS HALT indicator extinguishes and the ACTIVE indicator illuminates.
- 117. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates and the ACTIVE indicator extinguishes.
- 118. Observe that the BUS INDICATOR does not display 00000000.

THE FOLLOWING PROCEDURES TEST THE READ PUSHBUTTON SWITCH FUNCTION

- 119. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 120. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 121. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00045000.
- 122. Set the OPERATIONAL CONTROL rotary switch to CMPT.

- 123. Set the RUN/ONE INSTR toggle switch to RUN.
- 124. Press the INITIATE pushbutton switch and observe that the ACTIVE indicator illuminates.
- 125. Press the READ and NORMAL HALT pushbutton switches, in turn, and observe that the BUS INDICATOR displays a reading of 00045002.
- 126. Set the REGISTER SELECT rotary switch to CPS and observe that bit 12 of the BUS INDICATOR display equals 1.

THE FOLLOWING PROCEDURES TEST THE IMMEDIATE HALT SWITCH FUNCTION

- 127. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 128. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 129. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00045000.
- 130. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 131. Set the RUN/ONE INSTR toggle switch to RUN.
- 132. Press the INITIATE pushbutton switch and then the IMMED HALT pushbutton switch and observe that the PRCS HALT indicator is illuminated.
- 133. Set the REGISTER SELECT rotary switch to SC1 and observe that the BUS INDICATOR displays some 1's from bits 00 through 18.
- 134. Set the REGISTER SELECT rotary switch to SC2 and observe that the BUS INDICATOR displays some 1's from bits 00 through 18.

THE FOLLOWING PROCEDURES TEST THE MEMORY PROTECTION FUNCTION

- 135. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator is illuminated.
- 136. Press the CLEAR pushbutton switch.
- 137. Set the MEMORY guarded switch to the PROTECTED position.
- 138. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 139. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 140. Set the ASR toggle switches to 160000.

NOTE

Memory page 1, location 20000.

- 141. Set the REGISTER SELECT rotary switch to MEM.
- 142. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00030707.
- 143. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 144. Press the INITIATE pushbutton switch and observe that the US INDICATOR displays a reading of 00045000.
- 145. Set the OPERATIONAL CONTROL rotary switch to STORE SEQL and the REGISTER SELECT to MEM.
- 146. Set the WSR toggle switches to 60137756.
- 147. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 60137756.
- 148. Set the OPERATIONAL CONTROL rotary switch to STORE AND THE REGISTER SELECT to PEX.
- 149. Set the WSR toggle switches to 00045000.
- 150. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00045000.
- 151. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 152. Set the RUN/ONE INSTR toggle switch to RUN.
- 153. Press the INITIATE pushbutton switch and observe that the PRGM HALT and ACTIVE indicators illuminate.

- 154. Press the NORMAL HALT pushbutton switch and observe:
 - a. PRCS HALT indicator illuminates.
 - b. PRGM HALT and ACTIVE indicators extinguish.
- 155. Set the REGISTER SELECT rotary switch to CPS and observe that BUS INDICATOR bit 07 equals 1.
- 156. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- 157. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 158. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00030707.

Section III. PROGRAMMED TAPE DIAGNOSTIC PROGRAM

THE FOLLOWING PROCEDURES WRITE ALL 1'S INTO MEMORY EXCEPT FOR LOCATION 15000

- 1. Set the OPERATIONAL CONTROL rotary switch to STORE SEQL and the REGISTER SELECT to MEM.
- 2. Set the MEMORY guarded switch to the UNPROTECTED position.
- 3. Set the RUN/ONE INSTR toggle switch to RUN.
- 4. Set the WSR toggle switches to all 7's.
- 5. Press and hold the COORDINATE pushbutton switch.
- 6. Press the INITIATE pushbutton switch and then simultaneously release both the INITIATE and COORDINATE pushbutton switches.
- 7. Observe that the ACTIVE indicator illuminates and the PRCS HALT indicator is extinguished.
- 8. Press the NORMAL HALT pushbutton switch and observe that:
 - a. ACTIVE Indicator extinguishes.
 - b. PRCS HALT indicator illuminates.
 - c. BUS INDICATOR displays a reading of 77777777.
- 9. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 10. Set the ASR toggle switches to 15000.
- 11. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 12. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 77777777.
- 13. Set the WDR toggle switches to 01234567.
- 14. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 15. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 01234567.
- 16. Set the REGISTER SELECT rotary switch to PEX.
- 17. Set the WSR toggle switches to 00000400.
- 18. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00000400.
- 19. Set the OPERATIONAL CONTROL rotary switch to STORE SEQL and the REGISTER SELECT to MEM.
- 20. Set the WSR toggle switches to the instruction word settings shown in Table XXX, in sequence, and press the INITIATE pushbutton switch after each setting. Observe that the BUS INDICATOR displays the indicated instruction word.

Table XXX

Instruction word	Address location
01202404	00000400
00000400	00000401
05200377	00000402
24000405	00000403
22000400	00000404
70100001	00000405
7000001	00000406
01202400	00000407
00000400	00000410
02200400	00000411
24000407	00000412
01202404	00000413
00000400	00000414
34000020	00000415
35000010	00000416
72000001	00000417
7400003	00000420
22000407	00000421
62500475	00000422
72100001	00000423
74100235	00000424
22000406	00000425
00000500	00000426

- 21. Set the REGISTER SELECT rotary switch to PEX and observe that the BUS INDICATOR displays a reading of 00000427.
- 22. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator is illuminated.
- 23. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 24. Set the WSR toggle switches to 00000400.
- 25. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00000400.
- 26. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A.
- 27. Set the WSR toggle switches to 51137754.
- 28. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays the instruction word readings indicated on Table XXX in step 20 above.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE OFF-LINE DIAGNOSTIC LEADER PROGRAM INTO MEMORY

- 29. Load the off-line diagnostic loader tape (SM-D-752126) on the paper tape reader.
- 30. Set the paper tape reader MODE SELECT toggle switch to STRIP and the PWR switch to ON.
- 31. Set the system status panel RESET SELECT TAPE READER toggle switch to ON.
- 32. Press the system status panel RESET pushbutton switch several times and observe that the diagnostic loader tape moves.
- 33. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 34. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 35. Observe that the BUS INDICATOR displays a reading of 00000427.
- 36. Set the WSR toggle switches to 00000400.

- 37. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00000400.
- 38. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 39. Set the RUN/ONE INSTR toggle switch to RUN.
- 40. Press the INITIATE pushbutton switch and observe that:
 - a. Off-line diagnostic loader tape starts to load into memory.
 - b. PRGM HALT indicator illuminates at the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00000427.
- 41. Rewind the diagnostic loader tape by setting the system status panel TAPE READ REWIND toggle switch to ON.

THE FOLLOWING PROCEDURES LOAD THE DIAGNOSTIC PROGRAM INTO MEMORY

- 42. Set the REAL TIME CLOCK guarded switch to the DISABLE position.
- 42.1. Set the PARITY ERROR toggle switch to OFF.
- 42.2. Set the CLOCK OPERATE CONTROL rotary switch to CONT.
- 42.3. Set the ADV-RPT toggle switch to ADV.
- 43. Set the system status panel CONTROL TRANSFER toggle switch to the DISABLE position.
- 44. Load the Bootstrap Diagnostic Program (SM-D-751714) and Maintenance Control Panel Diagnostic Program (SM-D-751718) tape reel on the paper tape reader.

NOTE

The two segment Bootstrap Diagnostic Program must be loaded into memory prior to loading in the one segment Maintenance Control Panel Diagnostic Program.

- 45. Set the paper tape reader MODE SELECT toggle switch to REEL and the PWR switch to ON.
- 46. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates and the PRGM HALT indicator extinguishes.
- 47. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 48. Set the WSR toggle switches to 00000500.
- 49. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00000500.
- 50. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 51. Press the system status panel RESET pushbutton switch several times and observe that the diagnostic tapes move.
- 52. Press the INITIATE pushbutton switch and observe that:
 - a. Diagnostic program tapes start to load into memory.
 - b. PRGM HALT indicator illuminates at the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00000631.
- 53. Press the INITIATE pushbutton switch for a total of three (3) times and verify that the same indications obtained in step 52 above are observed.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE STARTING ADDRESS INTO MEMORY

- 54. Press the NORMAL HALT and the CLEAR pushbutton switches.
- 55. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- 56. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 57. Set the ASR toggle switches to 00011314.
- 58. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00042000.
- 59. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 60. Set the WSR toggle switches to 00047000.
- 61. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00047000.

- 62. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT Indicator illuminates and the PRGM HALT indicator extinguishes.
- 63. Press the CLEAR pushbutton switch and observe that the BUS INDICATOR displays all 0's.
- 64. Set the REGISTER SELECT rotary switch to PEX.
- 65. Set the WSR toggle switches to 00010000.
- 66. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00010000.
- 67. Set the system status panel LOCAL PRINTER toggle switch to ON.
- 68. Press the system status panel RESET pushbutton switch.
- 69. Set the WSR toggle switches to all 0's.

THE FOLLOWING PROCEDURES ARE USED TO TEST A PROGRAM HALT

- 70. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 71. Set the RUN/ONE INSTR toggle switch to RUN.
- 72. Press the INITIATE pushbutton switch and observe that:
 - a. PRGM HALT indicator illuminates.
 - b. PRCS HALT indicator extinguishes.
 - c. ACTIVE Indicator is illuminated.
 - *d.* BUS INDICATOR displays a reading of 00010014.
 - e. MCP TEST message is generated on the page printer.

THE FOLLOWING PROCEDURES ARE USED TO TEST THE STORE SEQUENTIAL MODE

- 73. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00010055.
- 74. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00010214.

NOTE

If the BUS INDICATOR displays address 00010070, It indicates an error while reading all 1's from memory. If the BUS INDICATOR displays address 00010205, it indicates an error occurred reading location 15000 for 01234567. Memory Location 11313 will have the address at which the all 1's test failed.

THE FOLLOWING PROCEDURES ARE USED TO TEST THE WORD SWITCH REGISTER

- 75. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00010232.
- 76. Set the WSR toggle switches to all 7's.
- 77. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00010254.
- 78. Set the WSR toggle switches to all 0's.
- 79. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00010272.
- 80. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00010300.
- 81. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00010316.

THE FOLLOWING PROCEDURES ARE USED TO TEST THE CONTROL PANEL INSTRUCTION FUNCTION

- 82. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 83. Press the NORMAL HALT pushbutton switch and observe:
 - a. PRCS HALT indicator Illuminates.
 - b. PRGM HALT indicator extinguishes.

- 84. Set the WSR toggle switches to 55037774.
- 85. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR.
- 86. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00010317.
- 87. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 88. Set the RUN/ONE INSTR toggle switch to RUN.
- 89. Press the INITIATE pushbutton switch and observe that:
 - a. PRGM HALT indicator illuminates.
 - b. ACTIVE indicator illuminates.
 - c. BUS INDICATOR displays a reading of 00010324.
- 90. Set the WSR toggle switches to all 0's.

THE FOLLOWING PROCEDURES TEST THE REGISTER SELECT SWITCH FUNCTION

- 91. Press the INITIATE pushbutton switch and observe that:
 - a. PRGM HALT indicator illuminates.
 - b. DATA WORD indicator illuminates.
 - c. BUS INDICATOR displays a reading of 00010375.
- 92. Set the REGISTER SELECT rotary switch, in sequence, to each position listed in Table IX below and observe that the BUS INDICATOR displays the numerical value listed.

Table IX

REGISTER SELECT	BUS INDICATOR
rotary switch	readings
SBR	00037764
LSR	67405067
OAR	03607766
IAR	03607765
MO	00010375
MEM	0000000
PEX	00010375
PC	00010375
EOA	00010375
A	37750377
В	0000000
Q	37751377
IR	00010375
CPS	3x340x0x (NOTE)
CPD	37630200
BR	00000770
SHC	0000000
RTC	17737762
SC1	2000000
SC2	0000000

NOTE CPS bit 21 should equal 1.

93. Set the REGISTER SELECT rotary switch to PEX.

THE FOLLOWING PROCEDURES ARE USED TO TEST THE CLEAR FUNCTION

- 94. Press the INITIATE pushbutton switch and observe that:
 - a. ACTIVE indicator illuminates.
 - b. PRGM HALT indicator illuminates.
 - c. BUS INDICATOR displays a reading of 00010532.
- 95. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates and the PRGM HALT indicator extinguishes.
- 96. Press the CLEAR pushbutton switch.
- 97. Set the REGISTER SELECT rotary switch, in sequence, to each position listed in Table XV below and observe that the BUS INDICATOR displays the numeric value listed.

Table XV

REGISTER SELECT	BUS INDICATOR
rotary switch	readings
SER	0000000
LSR	0000000
OAR	00100000
IAR	00100000
MO	7777777
MEM	0000000
PEX	0000000
PC	0000000
EOA	0000000
A	0000000
В	0000000
Q	0000000
IR	0000000
CPS	0010000x (NOTE)
CPD	4000000
BR	0000000
SHC	0000000
RTC	0000000
SC1	0000000
SC2	0000000

NOTE

CPS bit 21 should equal 1.

THE FOLLOWING PROCEDURES ARE USED TO RESTORE THE PEX REGISTER

- 98. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 99. Set the WSR toggle switches to 00010532.
- 100. Press the INITIATE pushbutton switch and observe that:
 - a. PRGM HALT indicator illuminates.
 - b. BUS INDICATOR displays a reading of 00010532.
- 101. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 102. Press the INITIATE pushbutton switch and observe that:
 - a. ACTIVE indicator illuminates.
 - b. PRGM HALT indicator illuminates.
 - c. BUS INDICATOR displays a reading of 00010714.

THE FOLLOWING PROCEDURES TEST THE ONE INSTRUMENT ON FUNCTION

- 103. Press the NORMAL HALT pushbutton switch and observe that:
 - a. PRCS HALT indicator illuminates.
 - b. PRGM HALT and ACTIVE indicators extinguish.
- 104. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 105. Press the INITIATE pushbutton switch and observe:
 - a. PRGM HALT Indicator illuminates.
 - *b.* PRCS HALT indicator extinguishes.
 - c. BUS INDICATOR displays a reading of 00C715.
- 106. Set the RUN/ONE INSTR toggle switch to RUN.
- 107. Press the INITIATE pushbutton switch and observe that:
 - a. ACTIVE Indicator illuminates.
 - b. PRGM HALT indicator illuminates.
 - c. BUS INDICATOR displays a reading of 00011020.

THE FOLLOWING PROCEDURES TEST THE READ PUSHBUTTON SWITCH FUNCTION AND THE MEMORY PROTECT FUNCTION FOR BOTH PAGE 1 AND 2

108. Set the MEMORY guarded switch to the PROTECTED position.

- 109. Press the INITIATE pushbutton switch and then immediately the READ pushbutton switch.
- 110. Observe that the PRGM HALT indicator illuminates and the BUS INDICATOR displays a reading of 00011121.

THE FOLLOWING PROCEDURES TEST THE FUNCTION CODE AND THE ADDRESS SWITCH REGISTER

- 111. Set the MEMORY guarded switch to the UNPROTECTED position.
- 112. Set the function code to 77.
- 113. Set the ASR toggle switches to 377777.
- 114. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00011133.
- 115. Set the function code and the ASR toggle switches to all 0's.
- 116. Press the INITIATE pushbutton switch and observe:
 - a. PRGM HALT indicator illuminates.
 - b. BUS INDICATOR displays a reading of 00011200.

THE FOLLOWING PROCEDURES TEST THE REAL TIME CLOCK ENABLE SWITCH

- 117. Set the REAL TIME CLOCK guarded switch to the ENABLE position.
- 118. Press the INITIATE pushbutton switch and observe:
 - a. PRGM HALT indicator illuminates.
 - b. BUS INDICATOR displays a reading of 00011225.

THE FOLLOWING PROCEDURES TEST THE NORMAL HALT FUNCTION

- 119. Press the INITIATE and then the NORMAL HALT pushbutton switches and observe that the PRGM HALT. indicator extinguishes and then illuminates, and the ACTIVE indicator illuminates and then extinguishes.
- 120. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 121. Set the WSR toggle switches to 00011236.
- 122. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00011236.
- 123. Set the WSR toggle switches to all 0s.
- 124. Set the OPERATIONAL CONTROL to CMPT.
- 125. Press the INITIATE pushbutton switch and observe that:
 - a. PRGM HALT indicator illuminates.
 - b. BUS INDICATOR displays a reading of 00011256.
 - c. END OF MP TEST message is generated on the page printer.
- 126. Set the MEMORY guarded switch to the PROTECTED position.

Section IV. REPEATING THE PROGRAM SECTION OF THE DIAGNOSTIC PROGRAM

- 1. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 2. Set the REAL TIME CLOCK guarded switch to the DISABLE position.
- 3. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- 4. Set the ASR toggle switches to 20000.
- 5. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00020000.
- 6. Set the WSR toggle switches to all 7's.
- 7. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 8. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 77777777.
- 9. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 10. Set the ASR toggle switches to 160000.

- 11. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 22222222.
- 12. Set the OPERATIONAL CONTROL to STORE.
- 13. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays all 7's.
- 14. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 15. Set the ASR toggle switches to 260000.
- 16. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 33333333.
- 17. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 18. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays all 7's.
- 19. Proceed to step 54, Section III.

Section V. MAINTENANCE CONTROL PANEL BIT VERIFICATION

- 1. If the other Maintenance Control Panel ACTIVE indicator is illuminated, its CPS bit 23 equals 1 and bit 23 of the Maintenance Control Panel under test must equal zero. If the other Maintenance Control Panel ACTIVE indicator is extinguished, then bit 23 of the Maintenance Control Panel under test must equal 1.
- 2. If the other Maintenance Control Panel and processor are ON LINE and operating properly, i.e., no control transfer malfunctions are occurring, its CPS bit 08 equals zero and bit 23 of the Maintenance Control Panel under test must equal zero.
- 3. If the other processor is OFF-LINE, display the CPS register and determine the value of CPS bits 08 and 23. For a valid test, the indicated bit values must agree with those defined in the following table.

MCP under test	Other MCP
Bit 22 = 0	Bit 08 = 0
Bit 22 = 1	Bit 08 = 1
Bit 23 = 1	Bit 23 = 0
Bit 23 = 0	Bit 23 = 1

Section VI. PROGRAMMED AND MANUAL TEST ERROR PRINTOUTS

Printout	Test description	Error vector XX =	Error	Logic associated with failure
MP01-XX ERROR STORE SEQUENTIAL LOC XXXXX PGE YY	Function: Store Sequential. Logic tested: CPH counter. OPS counter.	01	Where XXXXX is any location in memory and YY is page number, (except where XXXXX is 15000 when YY is OQ)	CPH, OPS, COMPW
	All memory locations checked preloaded to 77777777. Correct answer: All memory locations contain 777777777. Except page 0	02	Content not equal 77777777 Where XXXXX is 15000 and YY is 00.	OPS1, OPS2, SIP, MEM, STARTC
	address 1500 which contains 01234567.		Content not equal 01234567.	STRW

		Error		Logic
Printout	Test description	XX =	Error	with failure
MP02-XX	Function: WSR toggle switch Logic tested: OPS counter. CPS counter. WSR toggle switch SET INPUTS.	01	Wrong answer.	TROWSR WSR 00- WSR 2
MP03-XX	Initial conditions: WRS toggle switch - 77777777. Correct answer: Location 037774 contains 777777777. Function: WSR toggle switch Logic tested: OPS counter. CPH counter. Word switch register	01	Wrong answer.	TROWSR WSROO-3
	Reset inputs. Initial conditions: WSR toggle switch = 00000000. Location 037774 contains 777777777. Correct answer: Location 037774 contains 00000000.			
MP05-XX	Function REGISTER SELECT rotary switch register set states.			DISH, CPB00IND- CPB23IND
	CPH counter. OPS counter. Register selection	01	(SBR) incorrect	SEL SBR
	Register display	02	(LSC) incorrect	SEL LSR
	Initial conditions: None	03	(OAR) incorrect	SEL OAR
		04 05	(IAR) incorrect (2000 (200000)	SEL IAR SEL MEM
	Correct one	00		
	Correct answer.	00	(Q) Incorrect	
	All actual register bits set.	10	(CP) Incorrect	
	Function	10	(CPD) Incorrect	
	CLEAD pushbutton switch	10	(DR) Incorrect	
	CLEAR pushbutton switch.	12	(RTC) Incorrect	
	Register clear states.	15	(A) Incorrect	
	Logic tested:	01	(A) incorrect	CLRSW
	OPS counter	02	(Ω) incorrect	
	CPH counter	02	(SBR) incorrect	
	Perister selection	03	(ISP) incorrect	
	Register display	05	(OAR) incorrect	
	Initial conditions:	06	(IAR) incorrect	
	Registers contained values listed.	07	(CPS) incorrect	
		10	(CPD) incorrect	
		11	(BR) incorrect	
		12	(RTC) incorrect	

Printout	Test description	Error vector XX –	Error	Logic associated with failure
	Correct answer: All actual stages cleared. (With the exception of CPD00 and CPS08.)		Liidi	With failure
MP07-XX	Function: ONE INSTR. CLA instruction	01	(A) ≠ 7777T77 or PEX ≠ 010715.	COMPW ONI
	Logic tested: CPH counter. OPS counter.			
	Initial conditions: (A) =00000007. Processor halted PEX = 010714.			
	Correct answer: (A) = 77777777. PEX = 010715.			
MP08-XX	Instruction: MEMORY guarded switch STR.	01	Incorrect data in (160000).	Write lockout.
	Logic tested: Memory unprotected. Initial conditions:	02 03 04	CPS07 was set. Incorrect data in (260000). CPS07 was set.	
	(160000) = 777777777. (260000) = 777777777. CPS07 = 0.			
	Correct answer: (160000) = 22222222. CPS07 = 0. (260000) = 333333333. CPS07 = 0.			
MP09-XX	Function MEMORY guarded switch.	01 02	CPS12 was not set. Data in (160000) was changed.	Memory lockout.
	Logic tested: Memory protect.	03 04	CPS07 was not set. Data in (260000) was changed.	
	Read Pushbutton switch.		changoai	
	Initial conditions: (160000) = 12222222. (260000) = 333333333. CPS07 = 0. CPS12 = 0. MEMORY guarded switch set to PROTECTED.			
	Correct answer: (16000) = 22222222. (260000) = 333333333. CPS07 = 1. CPS12 = 1.			

		Error		Logic
Printout	Test description	vector XX –	Frror	associated
XP10-XX	Function: Function Code and Address Switch Register. Logic Tested: Function code and ASR toggle switches and register. Initial conditions: Function code set to 77. Address switch resister set to 377777. Correct answer:	01	Wrong answer.	TROFCSW TROASR FC00-FC05 ASR07-ASR23
	(37756) = 77377777.			
MP10-XX	Function: Function Code and Address Switch Register.	02	Wrong answer.	TROFCSW TROASR FC00-FC05 ASR07-ASR23
	Logic tested: Function code and ASR toggle switches and registers.			
	Initial conditions: Function Code set to 00. Address Switch Register set to 000000. (37756) = 77377777.			
	Correct answer: (37756) = 00000000.			
MP10-XX	Function: Read only nature of Function Code and Address Switch Register.	03	Logical 1's read from register.	TROFCSW TROASR FC00-FC06 ASR07-ASR23
	Logic Tested: Write addressing and control; address switch register and function code register gates.			
	Initial conditions: Function code set to 00. Address Switch Register set to 000000. (A) = 77777777.			
	Correct answer: (37756 = 00000000. <i>Note:</i> the program attempts to write ones into the register.			
MP11-XX	Function: REAL TIME CLOCK guarded switch DISABLE.	01	Wrong answer.	DRTCSW STPCLK
	Logic tested: Real time clock control.			
20	Initial conditions: REAL TIME CLOCK guarded switch set to DISABLE.			

		Error		Logic
Printout	Test description	XX =	Error	with failure
	Correct answer: RTC = 00000000.			
MP11-XX	Function: REAL TIME CLOCK guarded switch ENABLE.	02	Wrong answer.	DRTCSW AIRTC
	Logic tested: Real time clock control.			
	Initial conditions: REAL TIME CLOCK switch set to ENABLE.			
	Correct answer: RTC = 0000000.			

EXHIBIT B

CENTRAL PROCESSOR DIAGNOSTIC PROGRAM

Section I. GENERAL

A total of 112 individual test procedures make up the Central Processor diagnostic program. Failure indications for a particular test occur as maintenance error printouts on the local page printer and Section IX contains a listing of the individual maintenance printouts.

Each test in the Central Processor diagnostic program has a number assigned to it which is stored in the OAR register. The particular test number and the equivalent name for each test are also included in the diagnostic procedure. The logic data flow diagram, provided as an aid in running the diagnostic program, consists of three more segments: detailed tests, an interrupt processor routine, and a control subroutine. The detailed tests were designed to report failures in mechanization- level functions. The interrupt processor routine was designed to report any hangups, halt or other unexpected error detectable by the interrupts and the control subroutine processes the user-assigned operating modes of the program.

To fully utilize the Central Processor diagnostic program, the reader must have a clear understanding of how the diagnostic program interrogates the WSR toggle switch settings (program options) and where the program halts are embedded in the program. The program halts designated on the logic data flow diagram represent points in the program where the user must decide on two different actions by either pressing the INITIATE pushbutton switch or by pressing the NORMAL HALT and then, in turn, the INITIATE pushbutton switch.

Section II. DIAGNOSTIC PROGRAM

THE FOLLOWING PROCEDURES ARE USED TO CONVERT THE OPERATIONAL PRELOADER PROGRAM TO THE OFF-LINE DIAGNOSTIC PRELOADER PROGRAM

- 1. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT Indicator illuminates.
- 2. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 3. Set the WSR toggle switches to 00277750.
- 4. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 5. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A.
- 6. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 7. Set the WSR toggle switches to 55137754.
- 8. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified in the o-line program preloader instruction entries chart below. If the entries do not agree, or are absent, the on-line program preloader instructions must be loaded into memory before proceeding. If the entries appearing in parenthesis on the chart are already loaded into memory, proceed to step 42 below.

Preloader Instruction Chart

Address	Instruction
00277750	01077751
00277751	00002404
00277752	05200377
00277753	24077755
00277754	22077750
00277755	70100000
00277756	7000001
00277757	01077760
00277760	00002400
00277761	02200040
00277762	24077757
00277763	01077764
00277764	00002404
00277765	34000020
00277766	35000010
00277767	7200001
00277770	7400003
00277771	22077757
00277772	62501776 (62500476)
00277773	72100001
00277774	74100107 (74100235)
00277775	22077756
00277776	0000000

- 9. Set the MEMORY guarded switch to the UNPROTECTED position.
- 10. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 11. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 12. Verify that the CLOCK OPERATE CONTROL rotary switch is in the CONT position.
- 13. Press the CLEAR pushbutton switch.
- 14. Set the WSR toggle switches to 00277750.
- 15. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 16. Set the OPERATIONAL CONTROL rotary switch to STORE SEQL and the REGISTER SELECT to MEM.
- 17. Set the WSR toggle switches to the instruction entries listed in the on-line preloader instruction chart and press the INITIATE pushbutton switch after each setting. Observe that the BUS INDICATOR displays the entered instruction.
- 18. Press NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator lights.
- 19. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 20. Set the WSR toggle switches to 00277750.
- 21. Press the INITIATE pushbutton switch and observe that BUS INDICATOR displays the address listed.
- 22. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A.
- 23. Set the WSR toggle switches to 55137754.
- 24. Press INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified on the chart.

NOTE

The following procedures will correct an erroneous address entered from the chart of specified addresses and instructions.

- a. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- b. Set the ASR toggle switches to the correct address.
- c. Press INITIATE pushbutton switch and observe that the BUS INDICATOR displays the correct address.
- d. Set the WSR toggle switches to the correct instruction number.
- e. Set the OPERATIONAL CONTROL rotary switch to STORE.
- f. Press INITIATE pushbutton switch and observe BUS INDICATOR displays the correct instruction.
- g. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- *h*. Press INITIATE pushbutton switch and verify that the BUS INDICATOR displays the correct instruction.
- 25. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 26. Set the MEMORY guarded switch to the UNPROTECTED position.
- 27. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- 28. Set the ASR toggle switches to 277772.
- 29. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62501776.
- 30. Set the WSR toggle switches to 62500476.
- 31. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 32. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62500476.
- 33. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 34. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62500476.
- 35. Set the ASR toggle switches to 277774.
- 36. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100107.
- 37. Set the WSR toggle switches to 741000235.
- 38. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 39. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100235.
- 40. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 41. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100235.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE OFF-LINE DIAGNOSTIC LOADER PROGRAM INTO MEMORY

- 42. Load the off-line diagnostic loader tape (SM-D-752126) on the paper tape reader.
- 43. Set the paper tape reader MODE SELECT toggle switch to STRIP and the PWR switch to ON.
- 44. Set the system status panel RESET SELECT TAPE READER toggle switch to ON.
- 45. Press the system status panel RESET pushbutton switch several times and observe that the loader tape moves.
- 46. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 47. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 48. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 49. Set the WSR toggle switches to 00277750.
- 50. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 51. Set the OPERATIONAL CONTROL rotary switch to CMPT.

- 52. Set the RUN/ONE INSTR toggle switch to RUN.
- 53. Press the INITIATE pushbutton switch and observe that:
 - a. Off-line diagnostic loader tape strip loads into memory.
 - b. PRGM HALT indicator illuminates at the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00277777.
- 54. Rewind the loader tape by setting the system status panel TAPE READER REWIND toggle switch to ON.
- 55. Set the PARITY ERROR HALT toggle switch to OFF.
- 56. Set the CLOCK OPERATE CONTROL rotary switch to CONT.
- 57. Set the ADV-RPT toggle switch to ADV.
- 58. Set the REAL TIME CLOCK guarded switch to the DISABLE position.
- 59. Set the MEMORY guarded switch to the UNPROTECTED position.
- 60. Set the CONTROL TRANSFER toggle switch to DISABLE.
- 61. Set the printer motor control bypass toggle switch to BYPASS.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE DIAGNOSTIC PROGRAM INTO MEMORY

- 62. Load the Central Processor Diagnostic Program tape (SM-D-751715) on the paper tape reader.
- 63. Set he paper tape reader MODE SELECT toggle switch to REEL and the PWR switch to ON.
- 64. Press the system status panel RESET pushbutton switch several times and observe that the diagnostic tape moves.
- 65. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates and the PRGM HALT indicator extinguishes.
- 66. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 67. Set the WSR toggle switches to 00000500.
- 68. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00000500.
- 69. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 70. Press the INITIATE pushbutton switch and observe that:
 - a. Diagnostic program tape loads into memory.
 - b. PRGM HALT indicator illuminates at the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00000631.
- 71. Set the REAL TIME CLOCK guarded switch to the ENABLE position.
- 72. St the CONTROL TRANSFER toggle switch to ENABLE.
- 73. Set the PARITY ERROR HALT toggle switch to ON.
- 74. Rewind the diagnostic program tape by setting the system status panel TAPE READER REWIND toggle switch to ON.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE STARTING ADDRESS INTO THE PROGRAM COUNTER

- 75. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT Indicator illuminates.
- 76. Press the CLEAR pushbutton switch.
- 77. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 78. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 79. Set the WSR toggle switches to 00010000.
- 80. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00010000.
- 81. Set the system status panel RESET SELECT LOCAL PRINTER toggle switch to ON.
- 82. Press the system status panel RESET pushbutton switch several times.
- 83. Set the RUN/ONE INSTR toggle switch to RUN.
- 84. Set the WSR toggle switches to all 0's.

THE FOLLOWING PROCEDURES ARE USED TO EXECUTE THE **DIAGNOSTIC PROGRAM**

- 85. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 86. Press the INITIATE pushbutton switch and observe that:
 - a. CP TEST message is generated on the page printer.
 - b. PRGM HALT indicator illuminates.
 - c. BUS INDICATOR displays a reading of 000100017.
- 87. Press the INITIATE pushbutton switch and observe that:
 - a. PRGM HALT indicator illuminates.
 - b. BUS INDICATOR displays a reading of 00120244.
- 88. Press the INITIATE pushbutton switch and observe that:
 - a. PRGM HALT indicator illuminates.
 - b. BUS INDICATOR displays a reading of 00020276.
 - c. END OF CP message is generated on the page printer.

NOTE

If the program halts at any other BUS INDICATOR reading or any maintenance error printouts occur before the END OF CP message is generated, troubleshoot the Central Processor Unit in accordance with standard procedures established a the operating site.

Section III. UNSCHEDULED PROCESSOR INTERRUPTS

1. If an unscheduled Interrupt occurs, the following error message is generated on the local page printer: YYYYYPGZZ, where, AT LOC

CP VVVV WW XXX

CP = Central Processor

VVVV = Tet name

WW = Vector Number

XXX = one of the following interrupts listed below or a group of interrupts that occurred.

Interrupt	Description	CPS	
DPE	Data Parity Error	01	
TTY	Teletype	04	
IPE	Instruction Parity Error	05	
ILI	Illegal Instruction	06	
WLV	Write Lockout Violation	07	
PRH	Program Halt	09	
ТМО	Time Out Condition	10	
RIO	Remote TTY	16	
UND	Undetermined		

YYYYYY = address at which the interrupt occurred. PGZZ = page number when the interrupt occurred.

- 2. If an unscheduled interrupt occurs with the inhibit printout option selected (WSRO1 = 1), the program will halt at address 21077. The address at which interrupt occurred will be stored in the accumulator.
- 3. Set the REGISTER SELECT rotary switch to position A and record the BUS INDICATOR reading. This is the exact address at which the Interrupt occurred.
- 4. Set the REGISTER SELECT rotary switch to OAR and record the BUS INDICATOR reading. Refer to Section IV, to determine the exact test number that was being executed a the time of interrupt.

- 5. Set the REGISTER SELECT rotary switch to CPS.
- 6. Set the WSR toggle switches to all 0's.
- 7. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 8. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays all 0's, except for bit 08.

Test no.	Test name	Test no.	Test name	Test no.	Test name	
1	KD01	47	KB04	115	KF22	
2	KD02	50	KB05	116	KF23	
3	KD03	51	KB06	117	KF24	
4	KD04	52	KB07	120	KF25	
5	KD05	53	KB08	121	KF26	
6	KD06	54	KB09	122	KF27	
7	KD07	55	KB10	123	KJ01	
10	KD08	56	KB11	124	KJ02	
11	KD09	57	KB12	125	KJ03	
12	KD10	60	KB13	126	KJ04	
13	KD11	61	KB14	127	KJ05	
14	KD12	62	KB15	130	KJ06	
15	KD13	63	KB16	131	KJ07	
16	KD14	64	KB17	132	KJ08	
17	KA01	65	KB18	133	KJ09	
20	KA02	66	KB19	134	EX01	
21	KA03	67	KF00	135	EX02	
22	KA04	70	KF01	136	EX03	
23	KA05	71	KF02	137	EX04	
24	KA06	72	KF03	140	EX05	
25	KA07	73	KF04	141	EX06	
26	KA08	74	KF05	142	EX07	
27	KA09	75	KF06	143	EX08	
30	KA10	76	KF07	144	EX09	
31	KA11	77	KF08	145	EX10	
32	KA12	100	KF09	146	EX11	
33	KA13	101	KF10	147	EX12	
34	KA14	102	KF11	150	EX13	
35	KA15	103	KF12	151	EX14	
36	KA16	104	KF13	152	EX15	
37	KA17	105	KF14	153	EX16	
40	KA18	106	KF15	154	EX17	
41	KA19	107	KF16	155	EX18	
42	KA20	110	KF17	156	EX19	
43	KA21	111	KF18	157	EX20	
44	KB01	112	KF19	160	EX21	
45	KB02	113	KF20			
46	KB03	114	KF21			

Section V. PROGRAM OPTIONS

Option 1 = WSR00 set:

This option is the controlling option bit for the diagnostic program. If WSR00 is set, there must also be another WSR bit selected from WSR01 through WSR06. *Option 2 = WSR01 set:*

This option inhibits the local page printer. It is to be always used in conjunction with option 3 below.

Option 3 = WSR02 set:

This option halts the program when an error is detected within a test. The error vector is stored in the IAR register and can be determined by setting the REGISTER SELECT rotary switch to the IAR position. The error vector number will be displayed on BUS INDICATOR bits 18 to 23. The OAR register contains the particular test number that was being executed when the error was detected. If the REGISTER SELECT rotary switch is set to PEX, the BUS INDICATOR will display the address of the halt plus 1.

There are several choices at this point for program operation:

a. The program can be continued by pressing the INITIATE pushbutton switch.

b. The test can be repeated by pressing the NORMAL HALT pushbutton switch and then the INITIATE pushbutton switch. If the error does not occur, the program will continue in its normal sequence; if the error (text missing) will halt as before.

c. The loop test option (2) below) can be selected to loop this test continuously and aid in isolating the error. Option 3 can remain in effect during the loop test but it is subject to the procedures used in testing as to whether it is left in effect when option 4 is selected.

Option 4 = WSR03 set:

The selection of this option will loop the selected test until the option bit is reset. This option is normally used when an error is found in a particular test and is only selected after it has been determined that there is an error.

Option 5 = WSR04 set:

This option is used when a subunit of the program is to be looped.

WSR toggle switch

Option 6 = WSR05 set:

This option halts the diagnostic program at the end of each test. The test number will be stored in the OAR register. There are several options available at this point:

a. To continue the program to the next test, press the NORMAL HALT and then the INITIATE pushbutton switches. This directs the program to continue to the next test in the program.

b. The test just completed can be repeated in two ways:

(1) Select option 4 above and press the INITIATE pushbutton switch.

(2) Press the INITIATE pushbutton switch and the program will repeat the same test and will halt at the same place. This is useful in determining if the sequence of tests is being executed in the proper order.

Option 7 = WSR06 set:

This option allows the diagnostic program to be looped continuously until WSR bit 06 is reset.

NOTE

A summary of the various options is given in the chart below.

Description

00	Enables options 01 through 06.
01	Inhibits printout on local page inter.
02	Halt on error.
03	Loop on individual test.
04	Loop on a group of tests for a particular set of logic. For example the entire KD counter
05	portion of the test.
06	Halt at end of each test.
	Loop on complete Central Processor diagnostics.

Section VI. TROUBLESHOOTING A HARD FAULT

The TEST DESCRIPTION column for the error message located in Section IX describes the failing instruction that should be executed as a control panel instruction from the Maintenance Control Panel. The acronym listed in the LOGIC ASSOCIATED WITH FAILURE column can be used to index into TM 11-5805-628-34-7 which contains the fan-out for each signal within the Central Processor.

THE FOLLOWING PROCEDURES EXECUTE THE FAILING INSTRUCTION AS A CONTROL PANEL INSTRUCTION

- 1. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR.
- 2. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 3. Set the WSR toggle switches to the particular instruction listed in the TEST DESCRIPTION column.
- 4. Set the RUN/ONE INSTR toggle switch to RUN.

- 5. Press the INITIATE pushbutton switch and observe that the ACTIVE indicator illuminates.
- 6. When the diagnostic program halts, select the desired program option and set the WSR toggle switches accordingly.

Section VII. TROUBLESHOOTING A TRANSIENT FAULT

- 1. Load the off-line diagnostic preloader program and the off-line diagnostic loader tapes as outlined in Section II above.
- 2. Set the WSR toggle switches to 70100000.
- 3. Set the REGISTER SELECT rotary switch to PEX.
- 4. Press the INITIATE pushbutton switch and wait r the transient fault to cause the PRGM HALT indicator to illuminate.
- 5. Record the reading displayed on the BUS INDICATOR.
- 6. Set the WSR toggle switches to 74000000.
- 7. Press the INITIATE pushbutton switch and wait for the transient fault to cause the PRGM HALT indicator to illuminates.
- 8. Record the reading displayed on the BUS INDICATOR. If the BUS INDICATOR reading does not agree with the reading recorded in step 5 above, repeat the procedure until a consistent halt address can be obtained.
- 9. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR.
- 10. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 11. Set the WSR toggle switches to the particular instruction listed in the TEST DESCRIPTION column.
- 12. Press the INITIATE pushbutton switch and observe that the ACTIVE indicator illuminates.

Section VIII. OPERATIONAL HALT TABLE

	Symbolic			Symbolic		
Location	Address	Test	Location	Address		Test
01006		WSR option selection	015410	KFER06	KF06	
010676	KDER01	KD01 Error halt	015444	KFER07	KF07	
010730	KDER02	KD02	015477	KFER08	KF08	
011003	KDER03	KD03	015533	KFER09	KF09	
011053	KDER04	KD04	015566	KFER10	KF10	
011112	KDER05	KD05	015622	KFER11	KF11	
011204	KDER06	KD06	015655	KFER12	KF12	
011253	KDER07	KD07	015711	KFER13	KF13	
011321	KDER08	KD08	015744	KFER14	KF14	
011367	KDER09	KD09	016000	KFER15	KF15	
011435	KDER10	KD10	016034	KFER16	KF16	
011504	KDER11	KD11	016070	KFER17	KF17	
011546	KDER12	KD12	016124	KFER18	KF18	
011632	KDER13	KD13	016160	KFER19	KF19	
011724	KDER14	KD14	016214	KFER20	KF20	
011770	KAER01	KA01	016250	KFER21	KF21	
012027	KAER02	KA02	016304	KFER22	KF22	
012066	KAER03	KA03	016340	KFER23	KF23	
012163	KAER04	KA04	016374	KFER24	KF24	
012222	KAER05	KA05	016430	KFER25	KF25	
012261	KAER06	KA06	016464	KFER26	KF26	
012360	KAER07	KA07	016521	KFER27	KF27	
012421	KAER08	KA08	016617	KJER01	KJ01	
012462	KAER09	KA09	016720	KFER02	KJ02	
012531	KAER10	KA10	016762	KJER03	KJ03	
012566	KAER11	KA11	017050	KJER04	KJ04	
012623	KAER12	KA12	017100	KJER05	KJ05	
012671	KAER13	KA13	017131	KJER06	KJ06	
012747	KAER14	KA14	01/15/	KJER07	KJ07	
013024	KAER15	KA15	017255	KJER08	KJ08	
013064	KAER16	KA10	017315	KJHL19	KJ09	
013127	KAER17	KA17	017334	EXERUI	EX01-01	
013164	KAER18	KA18	017347	EXERU2	EX01-02	
013232	KAER 19	KA19	017303		EX02-01	
013203			017400		EX02-02	
013331			017410	EXERUS	EX03-01	
013430	KBER02	KB02	017431	EXER07	EX04-01	
013535	KBER03	KB02	017462	EXER08	EX04-01	
013571	KBER04	KB04	017506	EXER09	EX05-01	
013655	KBER05	KB05	017531	EXER10	EX06-01	
013711	KBER06	KB06	017604	EXER11	EX07-01	
013755	KBER07	KB07	017631	EXER12	EX08-01	
014046	KBER08	KB08	017656	EXER13	EX09-01	
014155	KBER09	KB09	017703	EXER14	EX10-01	
014223	KBER10	KB10	017710	EXER15	EX11-01	
014257	KBER11	KB11	017755	EXER16	EX12-01	
014357	KBER12	KB12	020002	EXER17	EX13-01	
014414	KBER13	KB13	020027	EXER18	EX14-01	
014514	KBER14	KB14	020054	EXER19	EX15-01	
014551	KBER15	KB15	020101	EXER20	EX16-01	
014606	KBER16	KB16	020126	EXER21	EX17-01	
014677	KBER17	KB17	020153	EXER22	EX18-01	
014734	KBER18	KB18	020202	EXER23	EX19-01	
015021	KBER19	KB19	020226	EXER24	EX20-01	
015131	KFER00	KF00	020263	EXER25	EX21-01	
015166	KFER01	KF01	020275		End of CP T	est
015215	KFER02	KF02	020677	OPTHLT	Select WSR	options
015266	KFER03	KF03	021076	INTHLT	Interrupt ha	t
015321	KFER04	KF04	021264	ICLOB	I oo many ir	nterrupts
015355	KFER05	KF05				

Operational Halt Table - Continued

	Symbolic			Symbolic		
Location	Address	Test	Location	Address		Test
01006		WSR option selection	015410	KFER06	KF06	
010676	KDER01	KD01 Error halt	015444	KFER07	KF07	
010730	KDER02	KD02	015477	KFER08	KF08	
011003	KDER03	KD03	015533	KFER09	KF09	
011053	KDER04	KD04	015566	KFER10	KF10	
011000			015500			
011112		KD05	015022			
011204			015055			
011253	KDERU/	KD07	015711	KFER13	KF13	
011321	KDER08	KD08	015744	KFER14	KF14	
011367	KDER09	KD09	016000	KFER15	KF15	
011435	KDER10	KD10	016034	KFER16	KF16	
011504	KDER11	KD11	016070	KFER17	KF17	
011546	KDER12	KD12	016124	KFER18	KF18	
011632	KDER13	KD13	016160	KFER19	KF19	
011724	KDER14	KD14	016214	KFER20	KF20	
011770	KAER01	KA01	016250	KFER21	KF21	
012027	KAER02	KA02	016304	KFER22	KF22	
012066	KAFR03	KA03	016340	KFFR23	KF23	
012163	KAFR04	KA04	016374	KFFR24	KF24	
012222	KAER05	KA05	016430	KFER25	KF25	
012261	KAER06	KAOG	016464	KFER26	KF26	
012201			016521			
012300			010021			
012421	KAERUO		010017	KJERUI	KJ01	
012462	KAERU9	KA09	016720	KFERU2	KJUZ	
012531	KAER10	KA10	016762	KJER03	KJ03	
012566	KAER11	KA11	017050	KJER04	KJ04	
012623	KAER12	KA12	017100	KJER05	KJ05	
012671	KAER13	KA13	017131	KJER06	KJ06	
012747	KAER14	KA14	017157	KJER07	KJ07	
013024	KAER15	KA15	017255	KJER08	KJ08	
013064	KAER16	KA16	017315	KJHLT9	KJ09	
013127	KAER17	KA17	017334	EXER01	EX01-01	
013164	KAER18	KA18	017347	EXER02	EX01-02	
013232	KAER19	KA19	017365	EXER03	EX02-01	
013263	KAER20	KA20	017400	EXER04	EX02-02	
013351	KAFR21	KA21	017416	EXER05	FX03-01	
013430	KBER01	KB01	017431	EXER06	EX03-02	
013473	KBER02	KB02	017447	EXER07	EX04-01	
013535	KBER03	KB02	017462	EXER08	EX04-07	
013571	KBED04	KB04	017506		EX05-01	
012655			017521		EX06 01	
013033			017551			
013711		KB00	017604		EX07-01	
013755	KBERU/	KBU/	017631	EXER12	EX08-01	
014046	KBER08	KB08	017656	EXER13	EX09-01	
014155	KBER09	KB09	017703	EXER14	EX10-01	
014223	KBER10	KB10	017710	EXER15	EX11-01	
014257	KBER11	KB11	017755	EXER16	EX12-01	
014357	KBER12	KB12	020002	EXER17	EX13-03	
014414	KBER13	KB13	020027	EXER18	EX14-01	
014514	KBER14	KB14	020054	EXER19	EX15-01	
014551	KBER15	KB15	020101	EXER20	EX16-01	
014606	KBER16	KB16	020126	EXER21	EX17-01	
014677	KBER17	KB17	020153	EXER22	EX18-01	
014734	KBER18	KB18	020202	EXER23	EX19-01	
015021	KBER19	KB19	020226	EXER24	EX20-01	
015131	KFER00	KEOO	020263	EXER25	EX21-01	
015166	KEER01	KE01	020275			Tost
015215	KEER02	KE02	020273		Salact W/S	R ontions
010210			020077			
015200			021076		The man ha	dil intorrurt
015321			021204	ICLUB	100 many	merrupts
015355	KFERU5	KFU5				

Section IX. MAINTENANCE ERROR PRINTOUTS

a. KA Counter Tests.

		Error vector		Logic associated	Suggested further
Printout	Test description	XX=	Error	with failure	checks and remarks
CPKA 01-XX	instruction: RLL0 (35000000) Logic tested: Arithmetic unit A and Q Registers, KA sequence counter, Address Register decoder net- work AR (F) = 00. Initial conditions: (A) = -52341234. (KAOP1) (Q) = -52341234. Correct answer: (A) = -52341234 stored in ACCSAV. (Q) = -52341234 stored in INORGSAV	01 02	(A) ≠ -52341234	A Reg. inputs AMG- AZG-	ACC and ORG are unaffected since KA counter should skip from KAM 1 to KAM 4. Invalid enabling signals may be present at A Register clock gates. Check that KA sequence counter skips from KAM 1 to . KAM 4. If not, check that AR(F) = 00 is properly decoded.
		02	(Q) ≠ -52341234.	QRG INPUTS QMG- QZG-	Invalid enabling signals may be present at Q Register input gates. Check that KA sequence counter does not enter KAM 3.
		03	AR DECODER BIT(S) PICK UP	AR(F) = 00.	Perform = RLL0 Test that AR(F) 00 is decoded, also ACC and QRG are unaffected since KA counter should skip from KAM 1 to KAM 4. This is the sum of above error vectors indicating that both have occurred
CPKA02-XX	Instruction: RLL 1 (3500001). Logic tested: Arithmetic Unit A and Q Registers, KA sequence counter, shift register and shift counter decoder SHC = 77_8 . Initial conditions: (A) = -77777777. (KAOP2) (Q) = -77777777. Correct answer: (A) = -777777777 contained (KAOP2). in ACCSAV/(Q) = -777777777 stored in QRGSAV.	01	(CA) ≠ -77777777	SLA- INPUT gates to A Register.	A Register input gates receiving SLA signals fail to transfer all ONE's. Check that KA sequence counter enters state KAM 3 to generate SLA. Check that shift counter decoder generates SHC = 77.
		02	(Q) ≠ -77777777.	SLQ INPUT gates to Q Register.	Q Register input gates receiving SLQ signals fail to transfer all ONE's. Check that KA sequence counter enters state KAM 3 to generate SLQ.
CPKA03-XX	Instruction: RLL 1 (35000001).	03 01	(A) ≠	SLA- input	This is the sum of above error vectors indicating that both have occurred. A Register input gates
	Logic tested: Arithmetic Unit A and Q Registers, KA sequence counter.		00000000.	gates to A Register.	receiving SLA signals fail to transfer all ZERO's.

Maintenance Error Printouts - Continued.

		Error		Logic	Suggested further
Printout	Test description	XX=	Error	with failure	checks and remarks
	shift register and shift counter decoder SHC = 77_8 . Initial conditions: = 0 (A) = 00000000/. (Q) = 00000000. Correct answer: (A) = 00000000 contained in ACCSAV/. (Q) = 00000000 contained in ORGSAV/				Check that KA sequence counter enters state KAM 3 to general SLA.
		02	(Q) ≠ 000000000.	SLQ input gates to Q Register.	SLQ input gates receiving SLQ signals fail to transfer all ZERO's. Check that KA sequence counter enters state KAM 3 to generate SLQ.
		03			I his is the sum of the above error vectors indicating that both have occurred.
СРКА04-ХХ	Instruction: RLL 1 (35000001). Logic tested: Arithmetic Unit Q and A Register, KA sequence counter and Processor gate flip-flops AMG, AZG, OMG, OZG	01	A00 = 0	SAT00 AZG	A Register bit 00 fails in switch from ZERO to ONE on RLL instruction. Check A00 clock and shift left input gates.
	Initial Conditions (A) = 25252525. (KAOP3) (Q) = 25252525. Correct answer: (A) = -52525252. (KAOP4) (Q) = -52525252. Actual A Register answer contained in location KAW.	02	A Register bits through 22 fail to transfer proper ONE's/ ZERO's combination on RLL instruction.	SLA shift gates for bits A01 through A22 of A Register. Also all clock gates (AMG) for bits A01 through A22.	Display actual answer contained in KAW; then check affected gate(s).
		04 03, 05 06 and 07	A23 = 1	SAMG SH23	A Register bit 23 fails to switch from ONE to ZERO on RLL instruction. Check A23 clock and shift- left input gates. These are sums of above error vectors indicating that more than one have
		10	Q00 = 0 Q Register bit 00 fails to switch from ZERO to ONE on RLL instruction	SQT00 QZG	Q Register bit 00 fails to switch from ZERO to ONE on RLL instruction. Check Q00 clock and shift left input gates.
		20	Q Register bits 01 through 22 fail to transfer ONE's/ ZERO's combination RLL instruction.	SLQ shift gates fir bits Q01 through Q22 of Q Register. Also all clock gates (QMG) for bits Q01 through Q22.	Display actual answer contained in KAW; then check affected gate(s).

Maintenance Error Printouts - Continued.

Printout	Tool deparintion	Error vector	Error	Logic associated	Suggested further
Printout	i est description	40			cnecks and remarks
		40 10-17, 20-27, 30-37, 40-47, 50-57, 60-67 and 70-77	Q23 = 1	SQMG.	Q Register bit 23 fails to switch from ONE to ZERO on RLL instruction. Check Q23 clock and shift- left gates. These are sums of above error vectors indicating that more than one have occurred. For example, error vectors of 04, 10, and 20 are summed and a printout of 34 ₈ results.
CPKA05-XX Arithmetic Unit A and Q Regis- ters, KA sequence counter, shift regis- ter, and shift counter	Instructions: RLL 1 (37000001). Logic tested: None Initial conditions: (A) = -77777777. (KAOP2) (Q) = -77777777. Correct answer: (A) = -777777777 stand in ACCSAV/ (Q) = -77777777 stored in QRGSAV.	01	(A) ≠ -777777777.	SRA input gates to A Register.	A Register input gates receiving SRA inputs fail to transfer all ONE's. Check that KA sequence counter enters state KAM 3 to generate SRA. Check also that shift counter decoder generates SHC = 77.
decoder SHC = 77 ₈		02 03		SRQ input gates to Q Register.	Q Register input gates receiving SRQ signals fail to transfer all ONE's. Check that KA sequence counter enters state KAM to generate SRQ. This is the sum of above error vectors indicating that both have occurred
CPKA06-XX	Instruction: RRL 1 (37000001). Logic tested: Arithmetic Unit A and Q Registers KA sequence counter, shift counter and shift counter decoder SHC = 77. Initial conditions: (A) = 00000000. (Q) = 00000000. Correct answer: (A) = 00000000 contained in ACCSAV/. (Q) = 00000000 contained in QRGSAV.	01	(A) ≠00000000.	A00-23 shift right input gates.	A Register shift right input gates fail to transfer all ZERO's. Check that KA sequence counter enters state KAM 3 to generate SRA. Check also that shift counter decoder generates SHC = 77.
		02	(Q) ≠ 00000000.	Q00-23 shift right input gates	Q Register shift right input gates fail to transfer all ZERO's. Check that KA sequence counter enter state KAM 3 to generate SRQ. This is the sum of the above error vectors indicating that both have occurred.
		Error		Logic	
-----------	---	---	--	--	---
Printout	Test description	vector XX=	Error	associated with failure	Suggested further checks and remarks
СРКА07-ХХ	Instructions: ARL 1 (3700001). Logic tested: Arithmetic Unit A Register, KA sequence counter and Processor gate flip-flops AMG, AZG. Initial conditions: (A) = -52525252. (KAOP4) (Q) = -52525252. Correct answer: (A) = 252525252. (KAOP3) (Q) = 25252525. Actual A Register answer contained in KAW	01	A00 = 1.	SATOO AZG.	A Register bit 00 fails to switch from ONE to ZERO on RRL instruction. Check A00 clock and shift right input gates.
		02	A01 = 0.	SAT01 AMG.	A Register bit 01 fails to switch from ZERO to ONE on RRL instruction. Check A01 clock and shift right input gates.
		04	A Register bits 02 through 23 fail to transfer proper ONE's/ZERO's. combination on RRL instruction.	SRA shift gates for bits 02 through 23 of A Register. Also all clock gates to (AMG) for bits A02 through A23.	Display actual answer contained in KAW; then check affected gate(s).
		03, 05, 06 and 07			These are sums of the above error vectors indicating that more than one have occurred.
		10	Q00 = 1	SQT00	Check Q00 clock and shift-
		20	Q01 = 0	SQZG SQT01	Check Q01 clock and shift-
		40	Q Register bits 02 through 23 fail to transfer proper ONE's/ZERO's combination.	SQMG QRG INPUTS SQMG SRQ shift gates for bits 02 through 23 of Q Register. Also all clock gates (QMG) for bits Q02 through Q23.	right input gates. Display actual answer, then check affected gates.
		10-17, 20-27, 30-37, 40-47, 50-57, 60-67, 70-77			These are sums of the above error vectors indicating that more than one have occurred. For example, error vectors of 04, 10, and 20 are summed and an error vector of 34 ₈ results.
СРКА08-ХХ	Instructions: NRM SHCSAV (41010464).	01	Shift count not written into memory	A01, NRM/NRL MEMORY WRITE	Display contents of SHCSAV after NRM execution, then check associated logic.

Printout	Test description	Error vector XX=	Error	Logic associated with failure	Suggested further checks and remarks
	Logic tested: Arithmetic Unit A Register, KA Sequence counter. Shift counter and memory write logic. Initial conditions: (A) = 20000000. (KAOP7). Correct answer: 00000000.				
	Actual answer contained in SHCSAV.	77	Shift count incor- rectly written into memory.	SHC→B BYG Shift counter logic.	Display contents of SHCSAV following NRM execution; then check associated
СРКА09-ХХ	Instruction: NRM SHCSAV (41010464). Logic tested: Arithmetic Unit A Register, KA sequence counter, shift counter. Initial conditions: (A) = 10000000. (KAPO10). Correct answer: 00000001. Actual answer contained in SHCSAV	01	NRM decode or timing error, shift count not written into memory or SHC23 = 0.	SBYG-SHC. ADDER BIT23→CPB SHC23→CPB23.	Display contents of SHCSAV following NRM execution, then check associated logic.
		77	Shift counter logic failure, shift countered pick- ed up bits or shift counter decoder failed	A01 + 26 ₈ SHC → CPB 18-22.	Display contents of SHCSAV following NRM executing; then check associated logic.
CPKA10-XX	Instruction: NRM SHCSAV (41010464). Logic tested: Arithmetic Unit A Register, KA sequence counter shift counter. Initial conditions: (A) = 00040000. (KAOP11). Correct answer: 00000010. Actual answer contained in SHCSAV.	01	Bit dropped during shift operation. A02 output BAD; or instruc- tion does not terminate when number is normalized.	SLA- SAMG- A02	Display contents of SHCSAV following NRM execution, then check associated logic.
		02	NRM instruction terminates prior to required number of shifts.	A02 + 26	Display contents of SHCSAV following NRM execution, then check associated logic.
		77	Shift counter carry network failure.	SHC ₂₈ → CPB ₂₀ SHC → SHC ADDER Carries bits 23-23.	Perform NRM SHCSAV test third set NRM logic levels, SHC adder carry levels and SHC inputs to adder.
CPKA11-XX	Instruction: NRM SHCSAV (41010464). Logic tested: Arithmetic Unit A Register, KA sequence counter, shift counter, shift counter decoded. Initial conditions: (A) = 00000000. Correct answer: 00000027. Actual answer contained in SHC- SAV.	01	Shift counter decoder fails, shift counter does not count.	A02 + 26 A01-	Display contents of SHCSAV; then check associated logic.

Printout	Test description	Error vector	Frror	Logic associated with failure	Suggested further
		77	Shift counter carry	SHC → CPB	Display contents of SHCSAV:
СРКА12- <u>XX</u>	Instruction: NRL SHCSAV (42010464). Logic tested: Arithmetic Unit A and Q Registers KA sequence counter, shift counter, shift counter decoder. Initial conditions: (A) = 000000000. (Q) = 000000000. Correct answer: 00000056. Actual answer contained in SHCSAV.	01	network problem. Shift counter decoder failure or shift count not written into memory.	A01- A02 + 55	then check associated logic. Display contents of SHCSAV; then check associated logic.
		77	Shift counter carry network error.	SHC \rightarrow CPB and SHC \rightarrow SHC carry petwork	Display contents of SHCSAV; then check associated logic.
CPKA13- <u>XX</u>	Instruction: NRL SHCSAV (42010464). Logic tested: Arithmetic Unit A and Q Registers, KA sequence counter shift counter	01	NRL instruction failed to shift Q Register causing shift counter to count out at 55.	SQMG-	If SHCSAV contains 00000056, check SQMG gates and SLQ gates.
	and shift counter decoder. Initial conditions: (A) = 00000000. (Q) = 00020000. (KAOP12) Correct answer: 00000040. Actual answer contained in SHCSAV.	02	Instruction failed to normalize correct number of places, QRG → ACC shifts logic or shift counter decoder failed.	A02 + 55 SLQ- SQ23-	Perform: NRL SHCSAV last set of NRL logic levels shift counter adder carries (19, 20). Display contents of SHCSAV. contains 00000056 and (Q) ≠ 2000000 check associated logic.
		77	Shift counter carry network failure.	SHC → SHC Carry network.	Display contents of SHCSAV. If SHCSAV contains value other than 00000056 check associated logic
СРКА14- <u>XX</u>	Instruction: RLS 6 (34000006). Logic tested: Arithmetic Unit A and Q Registers, KA sequence counter, shift counter and shift counter decoder SHC = 77. Initial conditions: (A) = 01470707 (A5) (Q) = -36307070 (AG) Correct answer: -47070701 (A14ANS). Actual answer contained in ACCSAV.	01	Q Register changes contents during RLS instruction execution.	QRG GATES	Display contents of QRGSAV; then check associated logic.
		02 04	A00 to A23 transfer logic fail. A01 to A00 transfer gates fail.	A00 → A23 A01 → A00	Display contents of ACCSAV; then check associated logic. Display contents of ACCSAV; then check associated logic.

		Error vector		Logic associated	Suggested further
Printout	Test description	XX=	Error	with failure	checks and remarks
		10	KAM3 unique RLS functions fail.	AZG, AMG shift counter logic.	Display content of ACCSAV; then check associated logic.
		03, 05 06, 07/ 10 ₈ through 17 ₈			These are sums of the above error vectors indicating that more than one have occur- red. For example error vectors of 04 and 10 are summed and an error vector of 14 or esults
CPKA15-XX	Instructions: RRS 6 (36000006). Logic tested: Arithmetic Unit A and Q Registers KA sequence counter shift counter shift counter and shift counter decoder SHC = 77. Initial conditions: (A) = 36307070. (A6). (A) = 01470707. (A7) Correct answer: -70763070 (A15ANS). Actual answer contained in ACCSAV	01	Q Register changes content during RRS execution.	QRG GATES	Display content of QRGSAV; then check associated logic.
	Actual answer contained in AccoAv.	02	A23 to A00 transfer logic fails.	A23 → A00.	Display content of ACCSAV; then check associated logic.
		04	A00 to A01 transfer gates fail.	A00 → A01.	Display content of ACCSAV; then check associated logic.
		10 03, 05,	KAM 3 unique RRS functions fail.	AZG, AMG SRA SHC logic.	Display content of ACCSAV; then check associated logic. These are sums of the above
		10 through 17 ₈			error vectors indicating that more than one have occurred. For example, error vectors 04 and 10 are summed and an error vector of 14_8 results.
СРКА16-ХХ	Instruction: RLQ 9 (40000009). Logic tested: Arithmetic Unit Q Register KA sequence counter, shift counter, shift counter decoder SHC = 77 ₈ Initial conditions: (Q) = -41234567 (A16). Correct answer: 34567412 (A16ANS).	01	Q00 = 1	Q01 → Q00	Display contents of Q Register to determine actual answer; then check associated logic.
		02	Q23 = 1	Q00 → Q23	Display contents of Q Register to determine actual answer; then check associated
		04	Bits 02 through 23 of Q Register fail to transfer proper ONEs/ZEROs combination.	QMG, QZG SLG shift counter logic.	Display content of Q Register to determine actual answer; then check associated logic.

		Error		Logic	Oursessed at front to a
Printout	Test description	Vector XX=	Error	associated with failure	checks and remarks
	Instruction: SPS 15 (22000015)	06, 07	400 - 0	CBD 102	vectors indicating that more one have occurred.
CPKA17-XX	Instruction: SRS 15 (32000015). Logic tested: Arithmetic Unit A Register, K4 sequence counter shift counter, shift counter decoder SHC = 77. Initial conditions: (A) = -52345676 Correct answer: (A) = -40000123. Actual answer contained in ACCSAV.	01	A00 = 0.	0 → A01	bisplay contents of ACCSAV; then check associated logic.
		02	A23 = 0.	A22 → A23	Display content of ACCSAV; then check associated logic.
		04	Content of A02 through A22 incorrect.	AZG AMG SRA Shift counter logic.	Display content of ACCSAV, then check associated logic.
		03, 05, 06, 07			These are sums of above vectors indicating that more than one have occurred.
CPKA18-XX	Instruction: SRL 23 (33000023). Logic tested: Arithmetic Unit A and Q Registers, KA sequence counter shift counter and shift counter decoder. Initial conditions: -57654321 +0 (AN18) (A18) (A) = -57654321 (A18N). (Q) = 00000000. Correct answer: (Q) = -57654321. (A) = 00000000. Actual answers stored in ACCSAV and QRGSAV.	01	A00	GRD102 0 → A01	Display contents of ACCSAV; then check associated logic.
		02	Q00 = 1	A00 → Q00	Display content of QAGSAV; then check associated logic.
		04	Content of A23 does not transfer to Q01.	A23 → Q01	Display contents of ACCSAV and QRGSAV; then check associated logic.
		10 03, 05 06, 07/ 10-17 ₈	Q01 = 1	SRA SRQ SAC logic.	Display content of QRGSAV, then check associated logic. These are sums of the above error vectors, indicating that more than one have occurred
CPKA19-XX	Instruction: SLS0 (3000000). Logic tested: Arithmetic Unit A Register, OA Flip- Flop, KA Sequence counter.	01	(OA) = 1	0 → OA	Display content of SC1 Register and observe status of bit 17. If overflow flip-flop is set, check associated logic.

		Error vector		Logic associated	Suggested further
Printout	Test description	XX=	Error	with failure	checks and remarks
	 (A) = 00000000. Correct answer: (A) = 00000000/ overflow flip-flop OA is reset. 				
CPKA20-XX	Instruction: SLS2 (3000002). Logic tested: Arithmetic Unit A Register, KA Sequence counter shift counter. Initial conditions: (A) = -77777777 (MONES). Correct answer: (A) = -7777774. (ANS20) Actual answer contained in ACCSAV.	01	A Register contains wrong value.	SLS AMG 0 → A23	Display content of ACCSAV; then check associated logic.
		02	(OA) = 0	A01 → 0VF	Display content of SC1 Register and observe status of bit 17; then check associated logic.
СРКА21- <u>XX</u>	Instruction: SLL 24 (31000024). Logic tested: Arithmetic Unit A and Q Registers, KA Sequence counter, shift counter, shift counter decoder (SHC = 7). Initial conditions: (A) = 0000000 (A18). (Q) = -77654321. (A18NL). Correct answer: (A) = -77530642. (ANS18) (A) = -4000000. Actual answers contained in ACCSAV and QRGSAV.	01	A and Q Register contain incorrect values.	QRG gating and shift counter logic.	Perform SLL 24 verify SLL decode, and SLL Functions. Display content of QRGSAV; then check associated logic.
		02	OA = 0	A01 → 0A	Display content of SC1 Register and observe status of bit 17; then check associated logic.
		04 03, 05 06 and 07	A23 = 1	Q01 → A23	Display content of QRGSAV and ACCSAV; then check associated logic. These are sums of above error vector indicating that more than one have occurred.
		10	A00 = 0	Q00 → A00	Display content of ACCSAV; then check associated logic.
		20	(A) incorrect.	Shift counter logic on A Register shift left gating.	Display content of ACCSAV; then check associated logic.

b. KB Counter Tests.

		Error		Logic	• · · • ·
Printout	Test description	vector	Error	associated with failure	Suggested further
	Instruction: KB0P01 570 10220	01		SAZG	KBM1 CAM: 1 AZG failed
CFRD01-XX	Logic tested:	01	A00 = 1.	3720	Display content of bit 00 from ACCSAV, then check associated logic.
	Central processor A Register, A + B carry network and KB counter logic.	02	(A) = 0.	AMG A0S1 KBM2	KBMZ CAM: 1 ĂMG, 1A0S1 failed. A + B carry failed to occur or did not load into A Register.
	Initial conditions: (A) = -00000077 (KB0P05). (B) = -00007777 (KB0P01). Correct answer:	03	(A) = 00010076.	KBM1 SAMG	(AMG at KBM1 time failed; AMG at KBM2 time is at ONE level.)
	(A) = 00007777. stored in ACCSAV.	04	(A) = 00000077.	A0S1 SAMG KBM1 or KBM2	SAMG in both KBM1 time and KBM2 time appears to have failed.
		77	(A) ≠ 00007777.	Add network or data inputs to A Register.	Adder failure or timing function failure; see other error vectors.
CPKB02-XX	Instruction: CSM KB0P02 (50010221). Logic tested:	01	A00 = 0.	1 => Ã00, AZG	Display content of A00 from ACCSAV, then check associated logic.
	Central processor A + B Registers; KB counter logic.	02	(A) = -37777777.	AMG, KBM1	A Register should be cleared of 00007777 at KBM1 time.
	Initial conditions: (A) = 00007777, CSM (KB0P02) = 37770000.	77	A ≠ -3777.	Adder inputs A = 0, B = 1	Display content of ACCSAV, then check associated logic.
	Correct answer: (A) = 37770000 (KB0P03). Actual answer stored in ACCSAV.			A = 0, B = 0 Bits 01-11 12-23	
CPKB03-XX	Instruction: CLS KB0P05 (56010224). Logic tested:	01	A00 = 1.	SAZG SBZG SAT00	Display content of A00 from ACCSAV, then check associated logic.
	Central processor A and B Registers; A + B carry network; KB counter logic.	02	(A) = 00000777.	AMG, KB counter.	A Register should be cleared at KBM1 time.
	Initial conditions: (A) = -00000700 (KB0P04). CLS (KB0P05) = -00000077.	77	(A) ≠ 00000077.	Adder inputs A = 0, B = 0 A = 0, B = 1	A + B carry network failure display contents of ACCSAV, then check associated logic.
	Correct answer: (A) = 00000077. Actual answer stored in ACCSAV.			Bits 1-17 18-23	
CPKB04-XX	Instruction: CLS KB0P07 (56010226). Logic tested: Central processor A, B Registers; A	01	A00 = 0.	SAT 00 SBT00	Sign bit of A Register did not change. Display content of A00 from ACCSAV, then check associated logic.
	+ B carry network; KB counter logic. Initial conditions: (A) = 00700000 (KB0P06). CLS (KB0P07) = 37000000. Correct answer: (A) = -37000000.	77	(A) ≠ 37000000.	Adder inputs A = 0, B = 1 A = 0, B = 0	A + B carry network failure. Display content of ACCSAV, then check associated logic.

		Error		Logic	Suggested further
Printout	Test description	XX=	Error	with failure	checks and remarks
СРКВ05-ХХ	Actual answer stored in ACCSAV. Instruction: LGN MZERO (04010502). Logic tested:	01	The sign of the A Register is incorrect	$Bits 1-5 6-23 AZG B_0 => B_0 B_0 => A_0$	Sign of A Register did not change. Display content of A00 from ACCSAV, then
	Central processor A, B Registers; A + B carry network; KB counter logic. Initial conditions: (A) = 00000007 (KB0P09), LGN (MZERO) = -00000000.	02 03	This is the same problem as ERROR KB03-01. A00 = 1. (A) = 00000000. (A) = 00000006.	SAZG- SAT00 SBZG- SBT00- COMP- AMG	LGN-KBM1: B- => B failure LGN - KBM1: 1 AMG failure.
	Correct answer: (A) = +37777777. (PONES)	04	(A) = 00077777	BNG	KBM1 time.
	Actual answer stored in ACCSAV.	05	(A) = 37700000.	BYG	causing bits 1-8 of the B Register not to complement
		05			at KBM1 time. The BYG level is inoperative, causing bits 9-23 of the B Register not to complement at KBM1 time.
		77	A ≠ 37777777.	A + B carry network or B complement gate.	ONE or more bits of A Register are incorrect.
CPKB06-XX	Instructions: LBN PONES (04010503) Logic tested: Central processor A, B Registers;	01	A00 = 0.	B ₀₀ => B ₀₀ AZG/B00 => B00	A bit or bits of the A Register are in error. Display content of ACCSAV to determine failure area.
	A + B carry network; KB counter logic. Initial conditions: (A) = 37777777 (PONES) Correct answer: (A) = -00000000 (MZEROS). Actual answer stored in ACCSAV	77	A ≠ -00000000.	KB counter, B complement B → A transfer	
СРКВ07-ХХ	Instruction: ADDC 7777 (12207777). Logic tested:	01	(A) = 37760001.	A00 X B00	Display contents of ACCSAV, then check associated logic.
	A + B carry network; KB counter logic.	02	A = 00000001.	AS ● OF- gate, KBM counter.	Display content of ACCSAV, then check associated logic.
	 (A) = 37770000. (KB0P02), ADDC 7777. Correct answer: (A) = 37777777 (PONES) Actual answer stored in ACCSAV. 	77	A ≠ 37777777.	Adder inputs A = 1, B = 0 A = 0, B = 1 Bits 1-11 12-23	Display contents of ACCSAV to determine failure areas, then check associated logic.
СРКВ08-ХХ	Instruction: ADD PONES (12010503). Logic tested: Central processor A, B	01	A = -37777776.	A00 X B00	A failure in the exclusive OR circuit of the processor (A) + (B) carry network could

		Error		Logic	Our sector di facetta en
Printout	Test description	Vector XX=	Error	associated with failure	Suggested further checks and remarks
	Registers: (A) + (B) carry network; KB counter logic.	707-			yield this incorrect answer.
	Initial conditions: (A) = -3777777 (MONES), ADD + 37777777. (PONES).	02	(A) = -37777777.	SAS-, KB counter	ADD KBM1 A00 X B00: IAS failed
	(A STAD) Correct answer: (A) = -00000000. (MZEROS). Actual answer stored in ACCSAV.	03	(A) = +00000000.	AS • OF- SAZG	A double failure in the AS • OF -circuit allows the KB counter to sequence through its remaining states.
		04	(A) = -37700000.	BNG	Add • KBM1 • A00 X B00 1 BNG failed.
		05	(A) = -00077777.	BYG	ADD • KBM1 • A00 X B00: 1 BYG failed.
		77	(A) ≠ -00000000.	Processor (A) + (B) carry network/KB counter.	Processor (A) + (B) carry network failure; or B- complement gate failure; or timing function failure. See other error vectors.
CPKB09-XX	Instruction: ADDC 7777 (12207777).	01	(A) = +00000000.	ASOF- COMP-	KB counter fails to increment from KBMB to KBM4
	Logic tested: Central processor A, B Registers; (A) + (B) carry network; KB counter	02	(A) = -37774000.	TROACPB TRIBCPB SAMG A0S1	KBM3 or KBM5 functions failed.
	Initial conditions: (A) = $-00003777.$ (KBQP15)	03 04	(A) = 37704000. (A) = +00010000.	SBNG SBYG	KBM4 function failure. Failure of BYG at KBM3 time.
	(R) = +0007777. Correct answer: (A) = +00004000	05 06	(A) = +00000001. (A) = +00074001	COMP- SBYG	KBM4 function failure. Failure of the BYG level at KBM4 time
	Actual answer contained in ACCSAV.	07	(A) = -00004000.	SAT00	Failure in logic setting of bit bit A00 at KBM5 time.
		77	(A) ≠ +00004000	KBM counter, processor (A) + (B) carry network	B Register complement gate failure; adder failure or timing function failure
CPKP10-XX	Instruction: ADD PONES (12010503). Logic tested: Central processor A, B Registers; (A) + (B) carry network; KB counter logic. Initial conditions: (A) = 37777777 (PONES). (B) = 37777777 (PONES). Correct answer: (A) = +37777776 (KB0P19). Actual answer stored in ACCSAV.	01	A ≠ +37777776.	Adder inputs A = 1, B = 1 Bits A11	Adder failure or timing function failure. Check other error vectors.
	Instruction: Add KB0P40 (12010267). Initial conditions:	02		Adder inputs	Adder failure or timing function failure. Check other error vectors.
	 (A) = 25252525 (KB0P40) (B) = 25252525 (KB0P40). Correct answer: (A) = 12525252. Actual answer stored in ACCSAV. 			(A) ≠ 12525252 A = 1, B = 1 A = 0, B = 0 <i>Bits</i> Odd Even	

		Error		Logic associated	Suggested further
Printout	Test description	XX=	Error	with failure	checks and remarks
	Instruction: ADD KB0P41 (12010270). Logic tested: None. Initial conditions: (A) = 12525252 (KB0P41). (B) = 12525252 (KB0P41). Correct answer: (A) = 25252524 (KB0P43). Actual answer stored in ACCSAV.	04	(A) ≠25252524.	Adder inputs A = 1, B = 1 A = 0, B = 0 Bits Even Odd	Adder failure or timing function failure. Check other error vectors.
СРКВ11-ХХ	Instruction: ADD KB0P01	03, 05, 06, 07 01	A00 = 1.	A00 X B00	These represent the sum of above error vectors indicating that more than one have occurred. Sign bit failure. Check other
	(12010220).	01	100 - 11	SAT 00	error vectors.
	Logic tested: Central processor A, B Registers; (A) + (B) carry network; KB counter logic. Initial conditions: (A) = +00000000. (B) = -00007777 (KB0P01). Correct answer:	77	(A) ≠ -00007777.	SAZG B Register complement gates or adder.	 (A) + (B) carry network failure; or B-Register complement failure; or timing function failure. See other error vectors.
	(A) = -00007777 (KB0P01).				
CPKB12-XX	Instruction: ADM KB0P12 (13010233).	01 02	(A) = -37700000. A = -00077774.	SBZG- A00	Sign bit fails to change. ADM • KBM1 • A00 failure.
	(A) + (B) carry network; KB counter	03	(A) = 37700001	COMP-	ADM • KBM1 • A00 B- => B transfer level failure.
	Initial conditions: (A) = -00077776 (KB0P20).	04	(A) = -00000000.	SBNG	ADM • KBM1 • A00: 1 BNG failure.
	(B) = -37777776 (KB0P12). Correct answer:	05	(A) = 37600003.	SBYG	ADM • KBM1 • A00: 1 BYG failure.
	(A) = +37700000 (KB0P10).	06	(A) = 00077777.	SAS-	ADM • KBM1 • A00: 1 AS failure.
		77	(A) ≠ 37700000.	Adder inputs A = 0, B = 0 A = 1, B = 0 A = 0, B = 1 Bits 1-8 9-22 23	Adder failure or B register complement gate failure; or timing function failure. See other error vectors.
CPKB13-XX	Instruction: ADMC 1 132 00001.	01	(A) = +37767777.	A00	ADM - KBM1 - A00 failure.
	Logic tested: Central processor A, B Registers; (A) + (B) carry network; KB counter logic. Initial conditions: (A) = 37770000 (KB0P02). Actual answer stored in ACCSAV.	77	A ≠ 37770001.	Adder inputs A = 1, B = 0 A = 0, B = 0 A = 0, B = 1 Bits 1-11 12-22 23	Adder failure or timing function failure. See other error vectors.
СРКВ14-ХХ	Instructions: SUB KB0P13 (16010234).	01	(A) = -36700000.	A ₀ + B ₀	SUB • KBM1 • (A00 X B00) - failure.

		Error		Logic	Suggested further
Printout	Test description	XX=	Error	with failure	checks and remarks
	Logic tested: Central processor A, B Registers; (A) + (B) carry network; KB counter logic. Initial conditions: (A) = -37000000.	02 03	(A) = -00700000. (A) = +00777777.	SBT00- SBZG COMP- SBYG-	 B00 => B00 failure during KBM1 or 1 BZG failure. B- => B transfer level failure during KBM1 or 1 BYG failure.
	(A) = 00700000. Actual answer stored in ACCSAV.	04 05 06	$\begin{array}{l} (A) = -37000000.\\ (A) = -37077777.\\ (A) = +00000001.\\ A \neq +00700000 \end{array}$	SBNG- SAS- SBNG- Adder inputs	1 BNG failure during KBM1. IAS failure during KBM1 time. 1 BNG failure during KBM3 time. Adder failure: or B Register
					timing function failure; or timing function failure. See other error vectors.
CPKB15-XX	Instruction: SUBC 6 16200006. Logic tested:	01	(A) = +00000005.	SBT00-	B00 => B00 failure during KBM1.
	Central processor A, B Registers; (A) + (B) carry network; KB counter logic. Initial conditions: (A) = +00000001. Correct answer: (A) = -00000005 (KB0P30). Actual answer stored in ACCSAV	77	(A) ≠ -00000005.	(A) + (B) carry network	Adder failure or timing function failure. See other error vectors.
CPKB16-XX	Instruction: KB0P31 (16010256). Logic tested: Central processor A. B Registers:	01	(A) = +17770001.	A00 X B00	SUB • KBM1 • (A00 X B00) - failure during KBM1 time.
	 (A) + (B) carry network; KB counter logic. Initial conditions: (A) = +00007777. Correct answer: +20007777. (KB0P32). Actual answer stored in ACCSAV. 	77	(A) ≠ +20007777.	Adder inputs A = 0, B = 1 A = 0, B = 0 A = 1, B = 0 Bits 1 2-11 12-23	Adder failure or timing function failure. See other error vectors.
CPKB17-XX	Instruction: SBMC 7 15 2 00007.	01	(A) = +00000001.	SBZG- SBT00-	1 BZG, 1 B00 failure during KBM1 time.
	Central processor A, B Registers; (A) + (B) carry network; KB counter logic.	02	(A) = -37777771.	COMP-	B- => B transfer level failure during KBM1 time.
	Initial conditions: (A) = $+0000006$.	03	(A) = 37700001	SBNG-	SBM • KBM1 • A00: 1BNG failure.
	Correct answer: (A) = -00000001 (KB0P34).	04	(A) = -00077763.	SBYG-	SBM • KBM1 • A00: 1 BYG failure.
	Actual answer stored in ACCSAV.	05	(A) = +37777776.	SAS-	SBM • KBM1 • A00: 1 AS
		77	(A) ≠ -00000001	(A) + (B) carry network	Adder failure or timing function failure. See other error vectors.

Printout	Test description	Error vector XX=	Error	Logic associated with failure	Suggested further checks and remarks
CPKB18-XX	Instruction: SBMC 7 (152 00007).	01	(A) = -00000001.	A00	SBM • KBM1 • A00 - failure
	Logic tested: Central processor A, B Registers; (A) + (B) carry network; KB counter logic. Initial conditions: (A) = -00000006. Actual answer stored in ACCSAV.	77	(A) ≠ -00000015.	Adder inputs A = 0, B = 0 A = 1, B = 1 A = 0, B = 1 Bits 1-20 21, 22 23	during KBM1 time. Failure in CPKB18 not already tested. Adder failure or timing function failure. Check other error vectors.
CPKB19-XX	Instruction: Case 1: ADD KB0P41 (12010270). Case 2: ADD KB0P42 (12010271). Case 3: ADD PONES (12010503). Logic tested: Central Processor A, B Registers; (A) + (B) carry network; OA logic. Initial conditions: Case 1: (A) = $+25252525$ (KB0P40). Case 2: (A) = $+12525252$ (KB0P41). Case 3: (A) = $+0000001$. Correct answer: Case 1: (A) = $+37777777$. (PONES). Case 2: (A) = $+0000000$. Case 3: (A) = $+0000000$.	01	OA = 1 (Case 1)	OA and AS logic.	The OA flip-flop should not set since the values added cannot produce an overflow condition.
		02	(A) ≠ +37777777 (Case 1).	(A) + (B) carry network (Case 1).	Adder network failure. Display content of ACCSAV; then check associated logic
		04	OA = 1 (Case 2)	OA and AS logic.	The OA flip-flop should not set since the values added cannot produce an overflow condition
	Instruction:	10	(A) 00000000.	(A) + (B) carry network (Case 2).	Adder network failure. Display content of ACCSAV2, then check associated logic.
	Logic tested:	10	OA = 0 (Case 3).	AS • OF	OA flip-flop fails to set when adding 37777777 plus 1.
	Initial conditions:	03, 05, 06, 07, 11-17, and 21-27			These values represent sums of the preceding error vectors indicating that more than one have occurred.
	Correct answer:				

c. PEX Tests.							
Printout	Test description	Error vector	Error	Logic associated	Suggested further		
CPEX01-XX	Instruction: STR PEX (60037754). Logic tested: Central Processor page register and page register central logic. Initial conditions: CLA E0AX1/STR PEX, A = (E0AX1) = EXS01. Correct answer: PEX = EXS01	01	PEX fails to trans- fer (PEX ≠ EXS01).	EOAX SEOAX1A- REOAX2A	This test stores the address of EXS01 in the PEX with E0AX = 01.		
		02	E0AX01 ≠ 1	SE0AX1A- RE0AX2A	The E0AX register should have the page 1 bit set.		
CPEX02-XX	Instruction: STR PEX (60037754). Logic tested: Central processor page register and page register control logic. Initial conditions: CLA (E0AX2/STRPEX, A = (E0AX2) = EXS02. Correct answer: PEX = EXS02	01	Program counter fails to transfer address (PEX ≠ EXS02)	SE0AX2A- RE0AX1A	This test stores the address of EXS02 in PEX with E0AX = 2.		
		02	E0AX ≠ 2	SE0AX2A- RE0AX1A	The E0AX register should contain the page 2 value.		
CPEX03-XX	Instruction: STR PEX (60037754). Logic tested: Central processor page register and page register control logic. Initial conditions: CLAE0AX3/STR PEX, A = (E0AX3) = EXS03). Correct answer: PEX = EXS03.	01	Program counter fails to transfer to proper address (PEX ≠ EXS03).	SEOAX1A- SEOAX2A	This test stores address of EXS03 in PEX and verifies E0AX contents.		
		02	E0AX1, E0AX2 to ≠ 1, 1	SE0AX1A- SE0AX2A-	The E0AX bits are tested for the page 3 value.		
CPEX04-XX	Instruction: STR PEX (60037754). Logic tested: Central processor page register and page register control logic. Initial conditions: PEX = 00017443 CLAE0AX4/STR PEX. Correct answer: PEX = EXS04 A = (E0AX4) = EXS04	01	Program counter fails to transfer to proper address (PEX ≠ EXS04).	RE0AX1A RE0AX2A	Test verifies operation of PEX register.		
	A = (EUAA4) = EA304.	02	E0AX1, E0AX2, ≠ 0, 0	RE0AX1A RE0AX2A	Test verities E0AX bits can be reset.		
CEPX05-XX	Instruction: STR * PG1, 60120307, CLA * PG1, 55120307. Logic tested: Central Processor page control and indirect addressing logic. Initial conditions: Content of location specified by PG2 00010000 (P1LOC).	01	Contents of PG1 (00150000) are not correct.	E0AX SE0AX1B RE0AX2B.	Test is to verify the indirect addressing function and paging.		
CPEX06-XX	Correct answer: Instruction: STR * PG2, (60120311). CLA * PG2, (55120311).	01	Contents of PG2 (00240500) are correct.	Indirect addressing E0AX SE0AX2B. RE0AX1B.	Test verifies indirect address- ing and page access.		

		Error vector	_	Logic associated	Suggested further
Printout	Test description	XX=	Error	with failure	checks and remarks
CPEX07-XX	Central processor page control and indirect addressing logic. Initial conditions: Contents of location specified by PG2 = 00000500 (02LOC). Correct answer: Instruction: TSA * PG00 (26120315). Logic tested: Central processor page control and index/indirect logic. Initial conditions: (PG00) - TRU EX07R	01	PCS ≠ 00017572	RE0AX1C RE0AX2C	Test of indirect transfer from within page 0.
CPEX08-XX	(22017572). Correct answer: PCS = EX07R (00017572). Instruction: TSA * PG1S (26120317). Logic tested Central processor page control and index/indirect logic. Initial conditions:	01	PCS ≠ 00017617	E0AX, Indirect transfer RE0AX1C RE0AX2C	Test of indirect transfer from page 0 to page 1.
CPEX09-XX	 (PG1S) specifies page 1, location 00015000. Correct answer: PCS = 00017617. Instruction: TSA * PG2S (26120320). Logic tested: Central processor page control and index/indirect logic. 	01	PCS ≠ 00017644	RE0AX1C RE0AX2C	Test of indirect transfer from page 0 to page 2.
CPEX10-XX	 (PG2S) specifies page 2, location 000050000. Correct answer: PCS = 00017644. Instruction: TSA * PG1T (26120321). Logic tested: Central processor page control and index/indirect logic. Initial conditions: (PG1T) specifies page 1, location 	01	PCS ≠ 00155002	RE0AX1C PE0AX2C	Test of indirect transfer from page 0 to page 1.
CPEX11-XX	00015001. Correct answer: PCS = 00155002 (TRU EX10R). Instruction: TSA * PG12T (26120322). Logic tested: Central processor page control and g register logic. Initial conditions: (PG42T) specifies page 1 logation	01	PCS ≠ 00155005	RE0AX1C RE0AX2C	Test of indirect transfer from page 0 to page 1 to page 2.
CPEX12-XX	00015003. Correct answer: PCS = 00155005. Instruction: TSA * PG21T (26120323). Logic tested: Central processor page control and index/indirect logic.	01	PCS ≠ 00245005	RE0AX1C RE0AX2C	Test of indirect transfer from page 0 to page 2 to page 1.

		Error vector		Logic associated	Suggested further
Printout	Test description	XX=	Error	with failure	checks and remarks
CPEX13-XX	(PG21T) specifies page 2, location 00005003. Correct answer: PCS = 00245005. Instruction:	01	PCS ≠ 00245002	RE0AX1C	Test of indirect transfer from
	TSA * PG22T (26120324). Logic tested: Central processor page control and index/indirect logic. Initial conditions: (PG22T) specifies page 2, location 00005001. Correct answer:			RE0AX2C	page 0 to page 2 to page 2.
CPEX14-XX	PCS = 002450002. Instruction: TRU * PG1SA (22120314). TSA * (pg. 1) 5007(26155007). Logic tested: Central processor page control and index/indirect logic. Initial conditions: (PG1SA) specifies page 1 location 00015006. [5007 (page 1)] = TRU EX14R. Correct answer: PCS = 00155007	01	PCS ≠ 00155007	RE0AX1C RE0AX2C	Test of indirect transfer from page 0 to page 1 to page 0.
CPEX16-XX	Instruction: TRP * P2P (21120335). Logic tested: Central processor page control and index/indirect logic. Initial conditions: (A) = 77777777 (MONES) Correct answer: (A) = 00000000	01	Transfer occurred	KCIND- KCISUMA TRPT- XTRPT SE0AX1E, SE0AX2E RE0AX1E, RE0AX2E RE0AX2E RE0AXST1, RE0AXST2	The TRP* instruction tests the restore functions of E0AX => E0AXST => E0AX. The transfer should not occur.
CEPX15-XX	Instruction: TRU * PG2SA (22120313). TSA * (Pg. 2) 5007 (26245007). Logic tested: Central processor page control and index/indirect logic. Initial conditions: (PG2SA) specifies page 2, location 00005006. [5007 (page 2)] = TRU EX15R. Correct answer: PCS = 00245007.	01	PCS ≠ 00245007	RE0AX1C RE0AX2C	Test of indirect transfer from page 0 to page 2 to page 0.
CPEX17-XX	Instruction: TRN * PIP (23120333). Logic tested: Central processor page control and index/indirect logic. Initial conditions: (A) = 00000000. Correct answer: (A) = 00000000.	01	Transfer occurred	E0AX _{1,2} => E0AXST _{1,2} => E0AX _{1,2} SE0AX1E, SE0AX2E RE0AX2E RE0AX1E, RE0AX2E SE0AX22, RE0AXST1, RE0AXST2	Transfer should not occur since sign bit (A00) is positive.

		Error		Logic	
Printout	Tost description	vector	Error	associated	Suggested further
	Instruction:	01	Transfer occurred	FOAY	The transfer should not occur
	TR7 * P1P2 (24120334)	01		FOAXST	since A register contains all
	Logic tested:			KCINB-	ones
	Central processor page control and				
	index/indirect logic.				
	Initial conditions:				
	(A) = 77777777.				
	Correct answer:				
	(A) = 00000000.				
CPEX19-XX		01	OA = 1	EUAX	The transfer should not occur,
	IRY * P2P0A (25120336)			EUAXSI	since the OA (overflow A
	Central processor page control and			KCINC-	register) hip-hop should be
	index/indirect logic.				10301.
	Initial conditions:				
	OA = 0.				
	Correct answer:				
	OA = 0, no transfer.				
CPEX20-XX	Instruction:	01	PEX not correct	E0AX,	Test verifies indirect transfer
	IRU * P2PIRU (22120337)		(A) ≠ 00245015	REOAX1C,	from page 0 to page 2.
	Logic tested:			REUAX2C	
	index/indirect logic			SEUAXIC,	
	Initial conditions:			SEUANZO	
	(P2PTRU) specifies page 2 location				
	00005015.				
	[5015 (page 2)] = CLA PEX.				
	Correct answer:				
	(A) = 00245015.			50.07	
CPEX21-XX		01	Indirect transfer	EUAX	The test verifies the HLT
	HLI PIPHLI (00120341).		Tailed $(A) \neq 0.0155014$	EUAXSI	Instructions transfer to
	Central processor page control and		$(A) \neq 00155014$	SEDAX1C	page 1.
	index/indirect logic.			SE0AX1C, SE0AX2C	
	Initial conditions:			RE0AX1C.	
	(P1PHLT) specifies page 1, location			E0AXST _{1,2}	
	00015014.			=> BREQ ₇₈	
	[5014 (page 2)] = CLA PEX.			E0AXST _{1,2}	
	Correct answer:			=> E0AX _{1,2}	
	(A) = 00155014.				

d. KD Counter Lists.

		Error		Logic	
- • • •		vector	_	associated	Suggested further
Printout	lest description	XX=	Error	with failure	Checks and remarks
CPKD01-XX	Logic tested: AR to PC gating.	01 02	PC ≠ AA PCS ≠ DER 11	AR to PC gating. PC + 1 PCS transfer.	PC. PC + 1 save failed to execute
	PC to PCS transfer. BR gating.	03			properly. Combination of error vectors
	Initial conditions: BR = 00. AR = AA. Correct answer:				01 and 02.
	PCS (Loc 000004) = DER 11. PC = AA.				
CPKD02-XX	Instruction: TSA BB 260 BB. Logic tested:	01	PC ≠ BB	AR to PC gating.	TSA failed to transfer AR to PC.
	AR to PC gating. PC to PCS transfer. BR gating.	02	PCS≠DER 21		execute properly.
	BR 77 AR = BB	03	PC ≠ AA and PCS ≠ DER 21		TSA decode failed.
	Correct answer: PCS = (LOC 000774) = DER 21 PC = BB.				
CPKD03-XX	Instruction: TSA CC 260 CC. Logic tested: KD counter PC + 1 to PCS transfer. BR gating	01	EOA ≠ PCS	PC to B gating EOA = PCS BYG BR gating.	Intermediate check determined EOA not correct for PCS location.
	AR to PC gating. BYG, BZG, BNG. Initial conditions: BR = 0	02		BZG BNG	Upper nine bits of PCS not cleared by TSA at (KDM 3 time).
	PCS = 77777777. Correct answer: PCS = KDKHB PC = CC	03	EOA PCS and PCS0-8 not cleared		TSA decode failed.
CPKD04-XX	Instruction: STQ TLOC 620 TLOC.	01	TLOC ≠ 77777777	Q to B gating.	Possible Q to B or memory write cycle failure.
	STQ decode and operation.	02	TLOC 00 ≠ 0	BZG	Q0 to B0 gating failed.
	Q = -777777777	03	TLOC 09-23 ≠ 77777	BYG or bit transfer.	If bits 9-23 = 0 check BYG. If bits 9-23 ≠ 0 QRG or BREG bit(s).
	Correct answer: TLOC = 77777777	04		BNG or bit transfer.	Bits $1-8 = 0$ BNG. Bits $1-8 \neq 0$ QRG or BRG bit(s) failed.
CPKD06-XX	Instruction: EX TLOC540 TLOC.	01	A REG = 0	Memory access or B to A transfer.	Bit or bit(s) of ACC failed, on B to A transfer.
	Logic tested: A to B transfer B to A transfer Initial conditions:	02	A01- 23 ≠ 25252525	AMG	Sign is positive bit - failed in A01-23.
	A = 73777777 TLOC = 25252525	03	A00 ≠ 0	CPB to A or B to CPB AZG	Perform B to A transfer. Sign bit failed. Other bits may also be in error
	Correct answer: TLOC = 77777777 A = 25252525	04	TLOC = 00000000	A to B transfer or write memory.	No transfer direct from ACC to B register at KDM1.

Drintout	Test description	Error vector	Free	Logic associated	Suggested further
	lest description	AA=	Error	With failure	LDO decede feiled
CPKD05-XX		01	Q ≠ ///////	B to Q transfer.	LDQ decode falled.
	LDQ MONES 520 MONES	02	0.00 - 1		OZG or B00 to 0.00 bit failed
	B to O transfer	02	Q 00 ≠ 1		
	Initial conditions:	03	001-023	OMG or hit transfer	OBG in error: if $O(1-23) = 0$
	$\Omega = 0$	00	+ 37777777 nor		Q(123) = 0
	Correct answer:		all zeros.		QMG failure: if $Q(1-23) \neq 0 Q$
	Q = -77777777				stage failure.
	Instruction:	05	TLOC 00 ≠ 1	BZG	B register sign bit failed to set
					KDM1 derived logic.
	Logic tested:	06	TLOC 09-23	BYG	Bits (B ₉ - B ₂₃) failed KDM1
			<i>≠</i> 77777		derived logic.
	Initial conditions:	07	TLOC 01-08 ≠ 377	BNG	Bits (B ₀ - B ₈) failed KDM1
					derived logic.
	Correct answer:	01	TI 00 00 14		Cian hit dronp od
CFKD07-XX	Instruction. SWR TLOC 470 TLOC	01	1LOC 00 ≠ 1	WOR UU SBZG	Sigh bit dropped.
	$MSK (A_{-}O)$ and B to memory	02	Rite 0.22 → 77777	MSG (01-15) SBVG	Bit(s) 9-23 dropped, could be
	MSK (A-Q) and B to memory	02	DIIS 9-23 7 11111	10130 (01-13) 3010	MSK inputs or transfer
					levels
		03			Combination of error sectors
					01 and 02.
	Initial conditions:	04	Bits ₁₋₈ ≠ 377	MSK ₁₋₈	Bit(s) 1-8 dropped, could be
	TLOC = 0			SBNG	MSK inputs or transfer
	(Q Reg), (A Reg) = KDPAT3 =				logic.
	777777777.				
	Correct answer: TLOC = (KDRAT2) = 77777777777777777777777777777777777				
	1EOC = (RDFAT3) = TTTTTTTT.	05			Combination of error vectors
					01 and 04.
		06			Combination of error vectors
					02 and 04.
		07			Combination of error vectors
					01, 02 and 04.
CPKD08-XX	Instructions:	01	TLOC $00 \neq 0$	MSK 00	Sign bit picked up or transfer
	SMR TLUC 470 TLUC.	02		SBZG	logic. Bit(c) 0.22 picked up or
	MSK and B to memory	02	1LOC 09-23 ≠	SBVC	transfer logic
	More and b to memory.	03	00000	0010	Combination of error vectors
	Initial conditions:				01 and 02.
	ACC = 77777777	04	TLOC 1-8 ≠ 000	SBNG	Bit(s) 1-8 picked up or
	KDPAT3 = 77777777			MASK	transfer logic.
	TLOC = 0000000				
	Q = 00000000				
	Correct answer:	05			Combination of among stars
	1200 = 00000000	05			Of and Of
		06			Combination of error vectors
		00			02 and 04.
		07			Combination of error vectors
					01, 02 and 04.
CPKD09-XX	Instructions:	01	TLOC 00 = 1	MSK	MASK inputs open or SMK
	SMK TLOC 470 TLOC.			SBZG	transfer logic.
		00	TI 00 00 00	Write	MACK inputs on on CMK
	MSK (A - Q)	02	1LOC 09-23 ≠	MSK SBVC	transfer logio
	b => memory. Initial conditions:			write	
	(QRG) (ACC) = 77777777	04	TI OC 01-08 + 377	Write	MASK inputs open or SMK
	(TLOC) = 77777777.			SBNG	transfer logic.
	· · · / · · ·			MSK	
	Correct answer:				
	(KDPAT3) = 77777777.				
		l	I	I	l

		Error		Logic	
Deinstaust	Test description	vector	Francis	associated	Suggested further
		XX=	Error		Checks and remarks
CPKD01-XX	LMK TLOCK 270 TLOC. Logic tested: MSK B to A transfer.	02	A00 ≠ 0 A09-23 ≠ 00000	SAZG SBZG MSK00 SAMG SBYG MSK (9-23)	stuck on - should not change sign bit MSK = 0. Stuck on or MASK inputs to B bad, MASK occurs when it should not.
	Initial conditions: (TLOC) (QRG) = 77777777. (ACC)	03 04	A01 = 08 ≠ 000		Combination of error vectors 01 and 02. Stuck on or MASK input to B bad. MASK occurs when it should not.
	(ACC) = 00000000.	05 06 07			Combination of error vectors 01 and 04. Combination of error vectors 02 and 04. Combination of error vectors 01 02 and 04.
CPKD11-XX	Instruction: LMK TLOC 270 TLOC. Logic tested:	01	A ₀ ≠ 1	SAZG SBZG MSK00	B • Q inputs to B failed to MASK.
	MSK (B • Q) B to A transfer	02	A00-23 ≠ 77777	SAMG SBYG MSK (9-23)	B • Q inputs to B failed to MASK
	Initial conditions: A = 00000000. Q = 00000000.	03		- ()	Combination of error vectors 01 and 02.
	TLOC - 77777777.	04	A01-08 ≠ 377		B • Q inputs to B failed to MASK.
	KDPAT3 = 77777777.	05			Combination of error vectors 01 and 04.
		06 07			Combination of error vectors 02 and 04. Combination of error vectors
CPKD12-XX	Instruction: CLLC 77777. 512 77777.	01	A00 ≠ 0	AZG	01, 02 and 04. Test that ACC sign is cleared on literal operation (G = 2).
	KD counter 0 => A Reg Load QRG from B.	02	A01-23 ≠ 00000000	AMG	Test that all is cleared on literal operation (G = 2).
	Initial conditions: A = 77777777 (KDPAT3). Correct answer:	03	Q00 ≠ 0	B to Q transfer and control, QZG.	B to Q transfer levels KDM4 failed.
	(ACC) = 00000000. (QRG) = 00077777.	04	Q01-23 ≠ 00077777		0 to QSN failed.
CPKD13-XX	Instruction: CLL TLOC3 510 TLOC3.	01	A01-23 ≠ 25252525	AMG, KDM1, B to A transfer and control.	KDM1 • AMG failed.
	Logic tested: B to A transfer B to Q transfer EOA + 1 to AR gating. Initial conditions: (TLOC3) = 25252525 (TLOC4) = 65252525	02 03	A00 ≠ 0 Q00 ≠ 1	AZG and B0 to A0 transfer QZG, B to Q transfer, EOA +1 => AR.	KDM1 • AZG failed. KDM4 • QZG failed.

		Error		Logic	
- • • •		vector	_	associated	Suggested further
Printout	Test description	XX=	Error	with failure	checks and remarks
	Correct answer:	04	Q01-23 =	AMG, B to Q	KDM1• QMG failed.
	(ACC) = 25252525 (QRG) = 65252525		0000000	transfer and control.	
		05	Q01-23 ≠ 25252525	QMG B to Q transfer	B to Q KDM4 failed.
CPKD14-XX	Instruction: STL TLOC 610 TLOC.	01	TLOC = 0	A => B and write	STL • KDM1 transfer failed.
	Logic tested:	02		BZG A to B	Sign bit failed A to B at
	A to B transfer		$TLOC_0 = 0$	transfer and	KDM1.
	Q to B transfer		TLOC 00 ≠ 1	control.	
	AR + 1 to EOA and write	03	TLOC09-23 ≠ 77777	BYG A to B transfer and control.	Bits (9-23) BYG failed A to B at KDM1.
	Initial conditions: LOC = (MONES) (A) = 77777777 LOC = (KDPAT1)				
	(Q) = 25252525	04	TLOC01-08 ≠ 377	BNG A => B transfer and control.	Bits (1-8) BNG failed A to B at KDM1.
	Correct answer:				
	A and (TLOC) = 77777777				
	Q and (TLOC + 1) = 25252525	05	TLOC + = 0	Q to B transfer, AR + 1 => EOA, write, KD counter sequencing.	Transfer level at KDM4.
		06	TLOC + 1 ≠	BYG, BNG, BZG,	B gates failed at KDM4.
			25252525	BREG write.	

d. KJ Counter Lists.

		Error		Logic	
Printout	Test description	vector XX=	Frror	associated with failure	Suggested further checks and remarks
CPKJ01-XX	Instruction: LXA * 7, 1 (70 4 00007)	01		Will failure	
	Logic tested: Indirect addressing, KJ counter, LXA mechanization Initial conditions: BR = 0 LOC 0 = 00000077		LOC 000007 = 00000005		EOA was unchanged from initial value (n) derived from indirect operation.
	LOC 7 = 37000005 (KJ0P01) Correct answer:				
	LOC 0 = 00000005	02	LOC 00000 = 00000106	INI- INR- DEX-	Indexing occurred instead of indirect.
		03	LOC 00000 =	INR	Indirect failed.
		04	LOC 00000 =	INR-	Indexing and indirect both
		05	00007700 LOC 00000 =	DE <u>X</u> - TRDARCPB	occurred. Transfer out of AR failed
			+ 00000000	TRICPB	putting 0's into the B
		06	LOC 00000 = + 00000077	KJ Counter Write.	Failure to change contents of location 00000 could be due to XJ counter bypassing WRITE
		77	other error LOC 0 ≠ 00000005	other KS Counter logic.	Manually single-step instruction and check mechanization
CPKJ02-XX	Instruction: LXA 5, 2 (70 1 00005) Logic tested: KJ Counter, LXA with direct address- ing, B register clearing during instruction access. Initial conditions: BR = 3 LOC 00031 = 00000002 LOC 00032 = +00000000 LOC 00005 = 00200007 LOC 00000 = 00000002 A Reg = -37000006 Correct answer:	01	LOC 00032 ≠ 00000000	Indirect addressing.	Indirect addressing occurred when it shouldn't have.
	LOC 00031 = 00000005	02	1.00.00001		Denk 0 colocted instead of
		02	00000005	BR to CPB transfer.	Bank 3. BR either wasn't loaded with No. 3 or the BR to ROA transfer failed
		03	LOC 00030 = 00000005	(G07 • G08) to EOA transfer.	IR1 (LOC 30) selected instead or IR2 (LOC 31) G Register transfer failure.
		04	LOC 00000 =	CPB to EOA	EOA was cleared instead of loaded with address of IR
		05	LOC 00031 =	BYG	
		06	LOC 00031 = -00000005	BZG	Instruction access logic B cleared during state 10.

		Error		Logic	Suggested further
Printout	Test description	XX=	Error	with failure	checks and remarks
	•	07	LOC 00031 = 37000005	BNG	
		11	00000005	logic.	instruction and check mechanization.
CPKJ03-XX	Instruction: LXA 5, 6 (70 3 00005) Logic tested:	01		IDR- DEX-	Both indexing and indirect occurred.
	Addressing Logic and LXA instruction Initial conditions: LOC 00012 = 00000000 LOC 00013 = 0000002 LOC 00007 = 00200007 Correct answer: LOC 00013 = 00000005		LOC 12 = 00000007		
		77	LOC 13 ≠ 00000005	other KJ counter logic.	Manually single-step instruction and check mechanization.
CPKJ04-XX	Instruction: IXA * 7, 3 (72 6 00007) Logic tested: Address modification logic, IXA instruction	01		INI IDR DEX	Indexing occurred, indirect did not.
	KJ counter A0S2 Initial conditions: BR = 0 LOC 00002 = 00000007 LOC 00071 = 00000000 LOC 00007 = 00200070 Correct answer: LOC 00002 = 00000077		LOC 00002 = 00000025		
		02	LOC 00002 = 00000000	A0S2- EDA to CPB transfer	Input to B Reg at KJ04 time is all zero's.
		03	LOC 00002 = 00000002	EOAG	EOA gate failed to set at KJ03 time.
		04	LOC 00002 = 00000007	SBY write EOA to CPB transfer CPB to B transfer.	B Reg did not change at KJ04 time or write failed.
		05	LOC 00077 = 00000077	EOAG	EOA did not change at KJ05 time.
		77	LOC 00002 ≠ 00000077	other KJ counter logic.	Manually single-step instruction and check mechanization.
CPKJ05-XX	Instruction: JXA 70, 1 Logic tested: JXA with indirect addressing	01	PC = 0 Next instruction was missed, transfer	AIPC	PC was cleared. PC was present without data at KJ05 time.
	Initial conditions: BR = 05 (KJOP13) LOC 00050 = 00000007 LOC 00000 = (KJOP06) = TRV EVI Correct answer: PC should be incremented by one, not two		to loc 0 occurred.		KJOP 13 = 500000 for BR = 5
		77	PC + 2 occurred (next instruction was skipped).	COMP, SAOF, AOF, Timing Logic KJ Counter.	Failure in the JXA logic such that PC + 2 was loaded into program counter.

		Error		Logic	• · · · ·
Printout	Test description	vector	Error	associated	Suggested further
	Instruction: IXA * 2, 3 (74.6.00002)	77	PC failed to skip	PCG- AIPC indirect	Program counter should be
CPKJ06-AA	Instruction: JXA 2, 3 (74 6 00002) Logic tested: JXA, indirect addressing, (I) > E Initial conditions: BR = 05 LOC 2 = 200007 (KJOP03) LOC 52 = 37777774 (KJOP08) LOC 0 = KJOP07 = TRU EV 77A Correct answer: 37777774>7 PC skip.		PC falled to skip.	addressing.	incremented by 2 because content of location 52 (effective address) is greater than content of location 2 (index register).
CPKJ07-XX	Instructions: JXA 7, 1 (74 0 00007) Logic tested: JXA with (I) = E Initial conditions: BR = 05 LOC 50 = 00000007 LOC 0 = TRU EV 77B Correct answer: Program counter should increment by one (not skip).	77	Program counter did not increment by one.	SAS- Timing Logic AOF was set.	
CPKJ08-XX	Instruction: JXD * 2, 3 (76 6 00002) Logic tested: KJ Counter JXD Logic Initial conditions: BR = 05 LOC 2 = 0020007 (KJOP03) LOC 52 = 0000077 LOC 0 = TRU EV 77C Correct answer: Next instruction should be skipped	01	Next instruction was executed and LOC 00052 = 00077776	JXD Class 1	Indexing occurred indirect failed no PC skip resulted.
	LOC 52 = 00000070	02	LOC 00052 = 00077672	SAS- COMP- SYBG- K 103 counted	First B register complement.
		03	LOC 00052 = 00077726	KJ04, EOA	EOA Reg fails to change at AJ04 time.
		04	LOC 00052 = 00000000 Program counter incremented by two.	AOS2- TROEOACPB- COMP- COMP B, 3	Adder Failure (B + AR) B + AR Failure; second complement of B failed. Zero's stored in B register at KJ08 time. This could be caused by not compliment- ing B at KJ06 time, failure of EOAG at KJ07 time. Failure of the KJ counter, failure of the BYG at KJ08 time.
		05	LOC 00052 = 00000077 Program counter incremented by two.	TRIBCPB- SBYG- TROEOACPB- SARG- EOA => B	BREG = initial value (77 ₈); EOA should equal 70 ₈ , AR value re-added to B reg AR failed to clear. Failure to transfer EOA to B
		10	LOC 00052 =	BYG	reg at KJ05 time. Failure or BYG at KJ06 time.
		77	LOC 00052 = 00000070	Timing Logic KJ Counter.	Manually single-step instruction and check mechanization.

f. KF Counter Tests.

		Error		Logic	
Deinstaust	Test description	vector	Freen	associated	Suggested further
		XX=		with failure	checks and remarks
CPKF00-XX	Instruction: CR 1, 0, KFW, 0 (07000001/00010273). Logic tested: Central Processor A, B, AR and Shift Counter Register, KF sequence counter and KF Sequence Counter and KF Counter PC control logic. Initial conditions: (KFW) = 00000000 (A) = +12341234	01	AIPC at ONE level.	AIPC	Invalid increment of Program Counter. Display content of shift counter, then check associated logic.
	(KFOP1) Correct answer: (KFW) = 00000000	02	(A) ≠ +12341234	TROBCPB- TRIACPB-	Original content of A Register (KFOP1) failed to restore. Display content of location 001040₀, then check
	(A) = +12341234 (KFOP1)	04	A Register save failed.	TRIBA-	associated logic. Display content of memory location 001040 ₈ , then check associated logic.
		10	Bit selector save failed.	TRIEOACPB- SEOA14-, SEOA18-, SEOAG- and G08	Display content of memory location 001041 ₈ , then check associated logic.
		20	Bit selector save location contains ZERO.	TROGCPB- TRIEOACPB- SEOA14- SEOA18- SEOAG	Display content of memory location 0010418; then check associated logic.
		40	A Register and bit selector saves failed.	Memory Address logic.	Display contents of memory locations 001041 ₈ and 001040 ₈ ; then check associated logic.
		70	(KFW) ≠ 0	KF counter (State 1100)	Display content of location KFW, then check associated logic
CPKF01-XX	Instruction: CR 0, 0, KFW, 0 (07000000/00010273). Logic tested: Arithmetic Unit A, B, AR, and shift counter logic. KF sequence counter, KF Counter PC control logic and Bit Selector Decodes. Initial conditions: -25222525 (KFOP2) Correct answer: 25225252	01	AIPC at ONE level.	AIPC BS = 0	Invalid Increment of Program Counter. Display content of shift counter; then check associated logic.
	(KFOP7) Actual answer contained in KFW.	02	AIPC at ONE level. (KFW) ≠ 25225252	BS = 0 KF counter SLA and SRA	Manipulation using B22 • B23 shift operation failure. Display content of memory location KFW; then check associated logic.

		Error		Logic	
Printout	Test description	vector	Frror	associated with failure	Suggested further
	rest description	03		with failure	This represents the sum of the above error vectors indicating that both have failed
CPKF02-XX	Instruction: CR 2, 0, KFW, 0 (07000002/00010273). Logic tested: Central Processor A, B, AR and SHC Registers, KF sequence counter, KF counter PC control logic and bit selector Decodes. Initial conditions: 35252525 (KFOP3) Correct answer: 25252525 (KFOP8) Contained actual answer in location KFW.	01	(KFW) ≠ 25252525	BS = 0 KF counter SLA and SRA	Manipulation Failure using B22 • B23 shift operation. Display content of memory location KFW; then check associated logic.
CPKF03-XX	Instruction: CR 3, 0, ACC, 0 (07000005/06010273) Logic tested: Control Processor A, B, AR and Shift Counter Registers; KF Sequence Counter, and Bit Selector decodes. Initial conditions: -16525252 (KFOP5) Correct answer: -1252522 (KFOP9) Actual answer contained in QRG	01	(QRG) ≠ -12525252	B23 • B22	Manipulation Failure using B23 • B22 shift operation. Display contents of A Register; then check associated logic.
		02	A Register was not manipulated	AR = ACC	Display content of A Register; then check associated logic.
	Instruction: ISA 1 0 KEW 0	04	Register save location failure.	RS = 0	001041_8 ; then check associated logic.
	 (07000001/00010273) Logic tested: Central Processor A, B, AR and Shift Counter Registers; KF sequence counter, KF counter PC control logic and bit selector decodes. Initial conditions: -17777777 (KCFC1) Correct answer: -377777777 (KFOP6) Actual answer contained in KFW 		level	63 = 0	No skip condition. Display content of shift counter; then check associated logic.
		02	(KFW) ≠ -37777777	BS = 0	SHC22 • A01: 1 A01 Function Failed. Display content of KFW; then check associated logic.

		Error		Logic	
Printout	Test description	vector	Frror	associated	Suggested further
CPKF05-XX	Instruction: CS 1. 0 KFW. 0	01	AIPC is at the ONE	BS = 0	AIPC Error SHC20 • SHC21
	(07000001/03010273) Logic tested: Central Processor A, B, AR and Shift Counter Registers; KF sequence counter, KF counter, PC control logic and bit selector decodes. Initial conditions: 20000000 (KCF1) Correct answer: 20000000 (KCF1)		level		 a) Shozo a Shozo
	Actual answer contained in KFW	00			
		02	(KEW) ≠ 20000000	B2 = 0	content of KFW; then check associated logic.
CPKF06-XX	Instruction: JSA 5, 0, KFW, 0 (07000005/00010273) Logic tested: Central Processor A, B, AR and shift counter registers; KF sequence counter, KF counter PC control logic and bit selector decodes. Initial conditions: -36777777 (KCPC5) Correct answer: -37777777 (KFOPG)	01	AIPC is at the ONE level.	BS = 1	AIPC error A05 • 21 = 0. Display content of shift counter; then check associated logic.
	Actual answer stored in KFW.	02	(KFW) ≠ 37777777	BS = 1	SHC22 • A05 = 1A05. Function failed. Display content of KFW; then check associated logic.
CPKF07-XX	Instruction: CS 5, 0, KFW, 0 (07000005/03010273) Logic tested: Central Processor A, R, AR and shift counter register. KF sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: 01000000 (KCF5) Correct answer: 01000000 (KCF5) Actual answer contained in KFW.	01	AIPC is at the ONE level.	BS = 1	AIPC • SHC20 • SHC21 = 0. Display content of shift counter; then check associated logic.
		02	(KFW) ≠ 01000000	BS = 1	SHC23 • A05 = 1A05. Display content of KFW; then check associated
CPKF08-XX	Instruction: JSA 9, 0, KFW, 0 (07000011/06010273)	01	AIPC is at the ONE level.	BS = 2	AIPC error A09 • SHC21 = 0. Display content of shift counter; then check associated logic.

		Error vector		Logic associated	Suggested further
Printout	Test description	XX=	Error	with failure	checks and remarks
	Logic tested: Central Processor A, B, AR, and shift counter registers; KF sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: -37737777 (KCFC9) Correct answer: -37777777 (KFOP6)				
	Actual answer contained in KFW	02	(KFW) + -37777777	BS = 2	$SHC22 \bullet A09 = 1A09$ function
		UL	(N W) + -3111111	50-2	failed. Display content of KFW; then check associated logic.
CPKF09-XX	Instruction: CS 9, 0, KFW, 0 (07000011/03010273) Logic tested: Central Processor A, B, AR and shift counter registers; KF sequence counter, KF counter PC control logic and bit selector decodes. Initial conditions: 00040000 (KCF9) Correct answer: 00040000 (KCF9) Actual answer contained in KFW.	01	AIPC is at the ONE level.	BS = 2	AIPC SHC20 • SHC21 = 0. Display content of shift counter; then check associated logic.
		02	(KFW) ≠ 00040000	BS = 2	SHC23 • A09 = 1A09 or test bit pickup of other normally "OFF" functions. Display content of KFW; then check associated logic.
CPKF10-XX	Instruction: JSA 12, 0, KFW, 0 (07000014/06010273) Logic tested: Central Processor A, B, AR and shift shift counter registers; KF sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: -37773777 (KCFC12) Correct answer: -377777777 (KFOP6) Actual answer contained in KEW	01	AIPC is at the ONE level.	BS = 3	AIPC error A12 • SHC21 = 0. Display content of shift counter, then check associated logic.
		02	(KFW) ≠ -37777777	BS = 3	SHC22 • A13 = IA13 function failed. Display content of KFW; then check associated logic.

		Error		Logic	
Printout	Test description	Vector XX=	Frror	associated with failure	Suggested further
CPKF11-XX	Instruction: CS 12, 0, KFW, 0 (07000014/03010273) Logic tested: Central Processor A, B, AR and shift counter, KF counter PC control logic and bit selector decodes. Initial conditions: 00004000 (KCF12) Correct answer: 00040000 (KCF12) Actual answer contained in KFW.	01	AIPC is at the ONE level.	BS = 3	AIPC SHC20 • SHC21 = 0. Display content of shift counter; then check associated logic.
		02	(KFW) ≠ 00040000	BS = 3	SHC23 • A13 = IA13. Display content of KFW; then check associated logic.
CPKF12-XX	Instruction: JSA 19, 0, KFW, 0 (07000023/06010273) Logic tested: Central Processor A, B, AR and shift counter registers; KF sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: -37777757 (KCFC19) Correct answer: -37777777 (KFOP6) Actual answer contained in KFW.	01	AIPC is at the ONE level.	BS = 4	AIPC error A19 • SHC21 = 0. Display content of shift counter; then check associated logic.
		02	(KFW) ≠ -37777777	BS = 4	SHC22 • A17 = IA17 function failed. Display content of KFW; then check associated logic.
CPKF13-XX	Instruction: CS 19, 0, KFW, 0 (07 19, 0/03 KFW, 0) Logic tested: Central Processor A, B, AR and shift counter registers; KF sequence counter, KF counter PC control logic and bit selector decodes. Initial conditions: +00000020 (KCF19) Correct answer: +00000020 (KCF19) Actual answer contained in KFW.	01	AIPC is at the ONE level.	BS = 4	AIPC error SHC20 • SHC21 = 0. Display content of shift counter; then check associated logic.
		02	(KFW) ≠ 00000020	BD = 4	SHC23 • A17 = IA17. Display content of KFW; then check associated logic.

		Error vector		Logic associated	Suggested further
Printout	Test description	XX=	Error	with failure	checks and remarks
CPKF14-XX	Instruction: JSA 23, 0, KFW, 0 (07000027/06010273) Logic tested: Central Processor A, B, AR and shift counter registers; KF sequence counter; KF counter PC counter logic and bit selector decodes. Initial conditions: -37777776 (KCFC23) Correct answer: -377777777 (KFOP6) Actual answer found in location KFW.	01	AIPC is at the ONE level.	BS = 5	AIPC error A23 • SHC21 = 0. Display content of shift counter; then check associated logic.
		02	(KFW) ≠ -37777777	BS = 5	SHC21 • A21 = IA21 function failed. Display content of KFW; then check associated logic.
CPKF15-XX	Instruction: CS 23, 0, KFW, 0 (07000027/03010273) Logic tested: Central Processor A, B, AR, and shift counter registers; KF sequence counter, KF counter PC counter control logic and bit selector decodes. Initial conditions: +0000001 (KCF23) Correct answer: +0000001 (KCF23)	01	AIPC is at the ONE level.	BS = 5	AIPC error/SHC20 • SHC21 = 0. Display content of shift counter; then check associated logic.
	Actual answer found in KFW.	02	(KFW) ≠ 00000001	BS = 5	SAC23 • A17 = IA17. Display content of KFW; then check associated logic.
CPKF16-XX	Instruction: JSR 1, 0, KFW, 0 (07000001/04010273) Logic tested: Central Processor A, B, AR and shift counter registers; KF sequence counter, KF counter PC control logic and bit selector decodes Initial conditions: -37777777 (KFOP6) Correct answer: -17777777 (KCFC1) Actual answer contained in KFW.	01	AIPC is at the ZERO level.	BS = 0	PC failed to skip SHC21 • A01 = AIPC. Display content of shift counter; then check associated logic.
		02	(KFW) ≠ -17777777	BS = 0	Test SHC23 • A01 inputs. Display content of KFW; then check associated logic.

		Error		Logic	
Printout	Test description	vector XX=	Frror	associated with failure	Suggested further
CPKF17-XX	Instruction: JRR 1, 0, KFW, 0 Logic tested: Central Processor A, B, AR and shift counter registers; KF sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: 00000000 (KFOP10) Correct answer: 00000000 (KFOP10) Actual answer contained in KEW	01	AIPC is at the ZERO level.	BS = 0	PC failed to skip SHC20 • A01-: AIPC. Display content of shift counter; then check associated logic.
		02	(KFW) ≠ 00000000	BS = 0	Test SHC22 • A01- inputs. Display content of KFW; then check associated logic.
CPKF18-XX	Instruction: JSR 5, 0, KFW, 0 (07000005/04010273) Logic tested: Central Processor A, B, AR and shift counter registers; KF sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: -377777777 (KFOP6) Correct answer: -367777777 (KCFC5) Actual answer contained in KFW.	01	AIPC is at the ZERO level.	BS = 1	PC failed to skip SHC21 • A05: AIPC. Display content of shift counter; then check associated logic.
		02	(KFW) ≠ -36777777	BS = 1	Test SHC23 • A05 inputs. Display content of KFW; then check associated logic.
CPKF19-XX	Instruction: JRR 5, 0, KFW, 0 (07000005/10010273) Logic tested: Central Processor A, B, AR and shift counter register; KF sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: 00000000 (KFOP10) Correct answer: 00000000 (KFOP76)	01	AIPC is at the ZERO level	BS = 1	PC failed to skip SHC20 • A05-: AIPC. Display content of shift counter; then check associated logic.
	Actual answer contained in KFW.	02	(KFW) ≠ 00000000	BS = 1	Test SHC22 • A05- inputs. Display content of KFW; then check associated logic.

		Error		Logic	Suggested further
Printout	Test description	XX=	Error	with failure	checks and remarks
CPKF20-XX	Instruction: JSR 9, 0, KFW, 0 (07000011/04010273) Logic tested: Central Processor A, B, AR and shift counter registers; KF sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: -37777777 (KFOP6) Correct answer: -37737777 (KCFC9)	01	AIPC is at the ZERO level.	BS = 2	PC failed to skip SHC21 • A09: AIPC. Display content of shift counter; then check associated logic.
		02	(KFW) ≠ -37737777	BS = 2	Test SHC23 • A09 inputs. Display content of KFW; then check associated logic.
CPKF21-XX	Instruction: JRR 9, 0, KFW, 0 (07000011/10010273) Logic tested: Central Processor A, B, AR and shift counter registers; KF sequence counter, KF counter PC counter logic and bit selector decodes. Initial conditions: 00000000 (KFOP10) Correct answer: 00000000 (KFOP10) Actual answer contained in KFW	01	AIPC is at the ZERO level.	BS = 2	PC failed to skip SHC20 • A09-: AIPC. Display content of shift counter; then check associated logic.
		02	(KFW) ≠ 00000000	BS = 2	Test SHC22 • A09- inputs. Display content of KFW; then check associated logic.
CPKF22-XX	Instruction: JSR 12, 0, KFW, 0 (07000014/04010273) Logic tested: Central Processor A, B, AR, and shift counter registers; KF sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: -377777777 (KFOP6) Correct answer: -37773777 KCFC12 Actual answer contained in KFW.	01	AIPC is at the ZERO level.	BS = 3	PC failed to skip SHC21 • A13: AIPC. Display content of shift counter; then check associated logic.
		02	(KFW) ≠ -37773777	BS = 3	Test SHC23 • A13 inputs. Display content of KFW; then check associated logic.
CPKF23-XX	Instruction: JRR 12, 0, KFW, 0 (07 12, 0/10 KFE, 0) Logic tested: Central Processor A, B, AR, and shift counter register; KF sequence counter; KF counter PC control logic and bit selector decodes.	01	AIPC is at the ZERO level.	BS = 3	PC failed to skip SHC20 • A13-: AIPC. Display content of shift counter; then check associated logic.

	Error		Logic	
Test description	Vector XX=	Error	associated with failure	Suggested further checks and remarks
00000000 (KFOP10) Correct answer: 00000000 (KFOP10)	701-			
	02	(KFE) ≠ 00000000	BS = 3	Test SHC22 • A13- inputs. Display content of KFW; then check associated logic.
Instruction: JSR 19, 0, KFW, 0 (07000023/04010273) Logic tested: Central Processor A, B, AR, and shift counter registers; KF sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: -37777777 (KFOP6) Correct answer: -37777757 (KCFC19) Actual answer contained in KFW	01	AIPC is at the ZERO level.	BS = 4	PC failed to skip SHC21 • A17: AIPC. Display content of shift counter; then check associated logic.
	02	(KFW) ≠ -3777757	BS = 4	Test SHC23 • A17 inputs. Display content of KFW; then check associated logic.
Instruction: JRR 19, 0, KFW, 0 (07000023/10010273) Logic tested: Central Processor A, B, AR and shift counter registers; KF sequence sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: 00000000 (KFOP10) Correct answer: 00000000 (KFOP10) Actual answer contained in KFW.	01	AIPC is at the ZERO level.	BS = 4	PC failed to skip SHC20 • A17: AIPC. Display content of shift counter; then check associated logic.
	02	(KFW) ≠ 00000000	BS = 4	Test SHC22 • A17- inputs. Display content of KFW; then check associated logic.
Instruction: JSR 23, 0, KFW, 0 (07000027/04010273) Logic tested: Central Processor A, B, AR, and shift counter registers; KF sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: -37777777 (kFOP6)	01	AIPC is at the ZERO level.	BS = 5	PC failed to skip SHC21 • A21: AIPC. Display content of shift counter; then check associated logic.
	Test description 00000000 (KFOP10) Correct answer: 00000000 (KFOP10) Actual answer contained in KFW Instruction: JSR 19, 0, KFW, 0 (0700023/04010273) Logic tested: Central Processor A, B, AR, and shift counter registers; KF sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: -37777777 (KFOP6) Correct answer: -377777757 (KCFC19) Actual answer contained in KFW Instruction: JRR 19, 0, KFW, 0 (07000023/10010273) Logic tested: Central Processor A, B, AR and shift counter registers; KF sequence sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: 00000000 (KFOP10) Correct answer: 00000000 (KFOP10) Correct answer: 00000000 (KFOP10) Actual answer contained in KFW. Instruction: JSR 23, 0, KFW, 0 (07000027/04010273) Logic tested: Central Processor A, B, AR, and shift counter registers; KF sequence counter; KF counter PC control logic and bit selector decodes. Initial	Test descriptionVector vector XX=00000000 (KFOP10) Correct answer: 0000000 (KFOP10) Actual answer contained in KFW02Instruction: JSR 19, 0, KFW, 0 (0700023/04010273) Logic tested: Central Processor A, B, AR, and shift counter registers; KF sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: -37777775 (KCFC19) Actual answer contained in KFW02Instruction: JRR 19, 0, KFW, 0 (07000023/10010273) Logic tested: Central Processor A, B, AR and shift counter registers; KF sequence sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: 0000000 (KFOP10) Correct answer: 0000000 (KFOP10) Correct answer: 0000000 (KFOP10) Correct answer: 0000000 (KFOP10) Actual answer contained in KFW.0101Instruction: JSR 23, 0, KFW, 0 (0700027/04010273) Logic tested: Central Processor A, B, AR, and shift counter registers; KF sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: 0000000 (KFOP10) Actual answer contained in KFW.0201Instruction: JSR 23, 0, KFW, 0 (0700027/04010273) Logic tested: Central Processor A, B, AR, and shift counter registers; KF sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: -3777777 (KFOP6)01	ErrorVectorXX=ErrorConcect answer: 00000000 (KFOP10) Actual answer contained in KFW02(KFE) \neq 00000000Instruction: JSR 19, 0, KFW, 0 (07000023/04010273) Logic tested: Central Processor A, B, AR, and shift counter registers; KF sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: -3777775 (KCP66)01AIPC is at the ZERO level.Context contained in KFW02(KFW) \neq .3777757(KFC19) Actual answer contained in KFW01AIPC is at the ZERO level.Control logic and bit selector decodes. Initial conditions: .37777757Instruction: JRR 19, 0, KFW, 0 (07000023/10010273) Logic tested: Control logic and bit selector decodes. Initial conditions: .0000000 (KFOP10)01AlPC is at the ZERO level.2Correct answer: .0000000 	Logic vector vectorEnd vector xX=Logic error00000000 (KFOP10) Correct answer: 00000000 (KFOP10) Actual answer contained in KFW02(KFE) \neq 00000000BS = 31Instruction: JSR 19, 0, KFW, 0 (0700002704010273) Logic tested: Correct answer: -3777777 (KFOP6)01AIPC is at the ZERO level.BS = 41Instruction: JRR 19, 0, KFW, 0 (0700002704010273) Logic tested: Correct answer: -377777501AIPC is at the ZERO level.BS = 41Instruction: JRR 19, 0, KFW, 0 (07000023/10010273) Logic tested: Control logic and bit selector decodes. Initial conditions: wolding and bit selector decodes. Initial conditions: (Correct answer: comotol (KFOP10) Actual answer contained in KFW.01AIPC is at the ZERO level.BS = 41Instruction: JRR 19, 0, KFW, 0 (07000027/04010273) Logic tested: Control logic and bit selector decodes. Initial conditions: wolding and bit selector decodes. Initial conditions: (Correct answer: 00000000 (KFOP10) Actual answer contained in KFW.01AIPC is at the ZERO level.BS = 41Instruction: JSR 23, 0, KFW, 0 (07000027/0410273) Logic tested: Control logic and bit selector decodes. Initial conditions: -3777777 (KFOP10)01AIPC is at the ZERO level.BS = 51Instruction: JSR 23, 0, KFW, 0 (07000027/0410273) Logic tested: -Control logic and bit selector decodes. Initial conditions: -3777777 (KFOP6)01AIPC is at the ZERO level.BS = 51Instruction: JSR 23, 0, KFW, 0 (07000027/0410273) Logic teste

		Error vector		Logic associated	Suggested further
Printout	Test description	XX=	Error	with failure	checks and remarks
	Correct answer: -37777776 (KCF23)				
		02	(KFW) ≠ -37777776	BS = 5	Test SHC23 • A21 input. Display content of KFW; then check associated logic.
CPKF27-XX	Instruction: JRR 23, 0, KFW, 0 (07000027/10010273) Logic tested: Central Processor A, B, AR and shift counter registers; KF sequence counter; KF counter PC control logic and bit selector decodes. Initial conditions: 00000000 (KFOP10) Correct answer: 00000000 (KFOP10) Actual answer contained in KFW.	01	AIPC is at the ZERO level.	BS = 5	PC failed to skip SHC20 • A21-: AIPC. Display content of shift counter; then check associated logic.
		02	(KFW) ≠ 00000000	BS = 5	Test SHC22 • A21- input. Display content of KFW; then check associated logic.



Figure 1 (1). Central processor Logic Data Flow Diagram (Sheet 1 of 6).



EL1UB002

Figure 1 (2). Central Processor Logic Data Flow Diagram (Sheet 2 of 6).



Figure 1 (3). Central Processor Logic Data Flow Diagram (Sheet 3 of 6).


Figure 1 (4). Central Processor Logic Data Flow Diagram (Sheet 4 of 6).



Figure 1 (5). Central Processor Logic Data Flow Diagram (Sheet 5 of 6).



Figure 1 (6). Central Processor Logic Data Flow Diagram (Sheet 6 of 6).

EXHIBIT C

MEMORY DIAGNOSTIC PROGRAM

Section I. GENERAL

The Memory diagnostic program is used to establish the veracity of the AN/TTC-38(V) electronic circuitry associated with the storage and retrieval of data. To assist maintenance personnel, the diagnostic program contains a sample listing of possible error messages (Section III) and the corrective action required.

The diagnostic program is executed in two parts: Segment A of the program is read into memory page zero (which also contains the loader programs) and is used to completely check memory pages 1 and 2. Segment B is initially read into memory page zero but after being entered, this segment (together with the loader programs, and any other contents of page zero) is read into memory page 2. This is done so that segment B of the program is positioned to execute a complete checkout of memory page zero.

Error printouts generated during the Memory diagnostic program employ a format which indicates the failed location and the type of error involved. For example, the page number can be determined from a six digit address such as BCDDDD, where:

(1) If C is 0 through 4, the address is on page 0.

(2) If C is 5 through 7, the page number is determined by B.

- (a) B = 0, page 0.
- (b) B = 1, page 1.
- (c) B = 2, page 2.

a. A typical memory write/mad error message is as follows: A-256321 W-7777777R-77773777, where:

A indicates page 2, memory address 16321.

W indicates an all ones (1's) pattern to be written into the addressed memory location.

R indicates the a one (1) was not read from bit 12 of the memory location.

b. A typical data parity error message is as follows: DPE XXXXXX, where:

DPE identifies a data parity error.

XXXXXX indicates the page and location of the program halt associated with the parity error.

The address and data involved with a data parity error printout is also identified by a write/read error printout. If the source of the program interrupt is other than a data parity error, the program will halt at address 00002601 for an illegal instruction or a instruction parity error or will halt at address 00002607 for all remaining interrupts. The accumulator will contain the address at which the interrupt occurred and the cause of the interrupt can be determined by examining the content of the CPS register.

Section II. DIAGNOSTIC PROGRAM

THE FOLLOWING PROCEDURES ARE USED TO CONVERT THE OPERATIONAL PRELOADER PROGRAM TO THE OFF-LINE DIAGNOSTIC PRELOADER PROGRAM

- 1. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 2. Set the OPERATIONAL CONTROL rotary switch to STORE AND THE REGISTER SELECT to PEX.
- 3. Set the WSR toggle switches to 00277750.
- 4. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 5. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A.
- 5.1. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 6. Set the WSR toggle switches to 55137754.

7. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified on the on-line program preloader instruction entries chart below. If the entries do not agree, or are absent, the on-line program preloader instructions must be loaded into memory before proceeding. If the entries appearing in parenthesis on the char are already loaded into memory, proceed to step 42 below.

Preloader Ir	nstructions	Chart
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Address	Instruction
00277750	01077761
00277751	00002404
00277762	05200377
00277763	24077755
00277764	22077750
00277755	70100000
00277756	7000001
002777n6	01077760
00277760	00002400
00277761	02200040
00277762	24077757
00277763	01077764
00277764	00002404
00277765	34000020
00277766	35000010
00277767	7200001
00277770	7400003
00277771	22077757
00277772	62501776 (62500476)
00277773	72100001
00277774	74100107 (74100235)
00277775	22077756
00277776	0000000

8. Set the MEMORY guarded switch to the UNPROTECTED position.

9. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.

10. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.

11. Verify that the RUN/ONE INSTR toggle switch is set to ONE INSTR.

- 12. Verify that the CLOCK OPERATE CONTROL rotary switch is in the CONT position.
- 13. Press the CLEAR pushbutton switch.
- 14. Set the WSR toggle switches to 00277750.

15. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.

16. Set the OPERATIONAL CONTROL rotary switch to STORE SEQL and the REGISTER SELECT to MEM.

- 17. Set the WSR toggle switches to the instruction entries listed in the on-line preloader instruction chart and press the INITIATE pushbutton switch after each setting. Observe that the BUS INDICATOR displays the entered instruction.
- 18. Press NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator lights.

19. Set the OPERATIONAL CONTROL rotary switch to Store and the REGISTER SELECT to PEX.

20. Set the WSR toggle switches to 00277750.

21. Press the INITIATE pushbutton switch and observe that BUS INDICATOR displays the address listed.

- 22. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A.
- 23. St the WSR toggle switches to 55137754.
- 24. Press INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified on the chart.

NOTE

The following procedures will correct an erroneous address entered from the chart of specified addresses and instructions.

- a. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- b. Set the ASR toggle switches to the correct address.
- c. Press INITIATE pushbutton switch and observe that the BUS INDICATOR displays the correct address.
- d. Set the WSR toggle switches to the correct instruction number.
- e. Set the OPERATIONAL CONTROL rotary switch to STORE.
- f. Press INITIATE pushbutton switch and observe BUS INDICATOR displays the correct instruction.
- g. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- *h.* Press INITIATE pushbutton switch and verify that the BUS INDICATOR displays the correct instruction.
- 25. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 26. Set the MEMORY guarded switch to the UNPROTECTED position.
- 27. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY AND THE REGISTER SELECT to MEM.
- 28. Set the ASR toggle switches to 277772.
- 29. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62501776.
- 30. Set the WSR toggle switches to 6500476.
- 31. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 32. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62500476.
- 34. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62500476.
- 35. Set the ASR toggle switches to 277774.
- 36. Press the INITIATE pushbutton switch and observe that the -BUS INDICATOR displays a reading of 74100107.
- 37. Set the WSR toggle switches to 74100235.
- 38. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 39. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 7410025.
- 40. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 41. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100235.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE OFF-LINE DIAGNOSTIC LOADER PROGRAM INTO MEMORY

- 42. Load the off-line diagnostic loader tape (SM-D-752126) on the paper tape reader.
- 43. Set the paper tape reader MODE SELECT toggle switch to STRIP and the PWR switch to ON.
- 44. Set the system status panel RESET SELECT TAPE READER toggle switch to ON.
- 45. Press the system status panel RESET pushbutton switch several times and observe that the leader tape moves.
- 46. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT Indicator illuminates.

- 47. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 48. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 49. Set the WSR toggle switches to 00277750.
- 50. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 51. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 52. Set the RUN/ONE INSTR toggle switch to RUN.
- 53. Press the INITIATE pushbutton switch and observe that:
 - a. Off-line diagnostic loader tape strip leads into memory.
 - b. PRGM HALT indicator illuminates at the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00277777.
- 54. Rewind the loader tape by setting the system status panel TAPE READER REWIND toggle switch to ON.
- 55. Set the PARITY ERROR HALT toggle switch to OFF.
- 56. Set the CLOCK OPERATE CONTROL rotary switch to CONT.
- 57. Set the ADV-RPT toggle switch to ADV.
- 58. Set the REAL TIME CLOCK guarded switch to the DISABLE position.
- 59. Set the MEMORY guarded switch to the UNPROTECTED position.
- 60. Set the CONTROL TRANSFER toggle switch to DISABLE.
- 61. Set the printer motor control BYPASS toggle switch to BYPASS.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE MEMORY DIAGNOSTIC PROGRAM INTO MEMORY

62. Load the Memory Diagnostic (SM-D-751716) and Memory-Memory and Control XFR (SM-D-751717) Diagnostic Program tapes on the paper tape reader.

NOTE

The three segments of the Memory-Memory and Control XFR diagnostic tape must be loaded into memory prior to leading the two segment Memory diagnostic tape.

- 63. Set the paper tape reader MODE SELECT toggle switch to REEL and the PWR switch to ON.
- 64. Press the system status panel RESET pushbutton switch several times and observe that the diagnostic tape move.
- 65. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates and the PRGM HALT indicator extinguishes.
- 66. St the OPERATIONAL CONTROL rotary switch to STORE.
- 67. Set the WSR toggle switches to 00000500.
- 68. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00000500.
- 69. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 70. Press the INITIATE pushbutton switch and observe that:
 - a. Diagnostic program tape loads into memory.
 - b. PRGM HALT Indicator illuminates at the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00000681.
- 71. Press the INITIATE pushbutton switch for a total of four (4) times to load the first segment (A) of the memory diagnostic tape and verify that the same indications obtained in step 70 above are observed.
- 72. Set the REAL TIME CLOCK guarded switch to the ENABLE position.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE STARTING ADDRESS INTO THE PROGRAM COUNTER

- 73. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 74. Press the CLEAR pushbutton switch.

- 75. Set OPERATIONAL CONTROL rotary switch to STORE.
- 76. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 77. Set the WSR toggle switches to 00002000.
- 78. Press the INITIATE pushbutton switch and observe that the BUS INDICTOR displays a reading of 00002000 (memory page 0, location 2000).
- 79. Set the system status panel LOCAL PRINTER toggle switch to ON and press the RESET pushbutton switch.
- 80. Set the WSR toggle switches to all 0's.

THE FOLLOWING PROCEDURES ARE USED TO TEST PAGE 1 AND 2 USING SEGMENT A IN PAGE ZERO

- 80.1 Set the MEMORY guarded switch to the UNPROTECTED position.
- 81. Set the OPERATIONAL CONTROL rotary switch to COMPT.
- 81.1 Set the RUN/ONE INSTR toggle switch to RUN.
- 82. Press the INITIATE pushbutton switch and observe the following after approximately 50 seconds.
 - a. PRGM HALT indicator illuminates.
 - b. BUS INDICATOR displays a reading of 00002507.
 - c. END MEM A message is generated on page printer.

THE FOLLOWING PROCEDURES ARE USED TO TEST PAGE ZERO: SEGMENT B IS LOADED INTO PAGE ZERO AND THEN TRANSFERRED TO PAGE 2

- 83. Press the NORMAL HALT and CLEAR pushbutton switches and observe that the PRCS HALT indicator is illuminated.
- 84. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 85. Set the WSR toggle switches to 00000506.
- 86. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays 00000506.
- 87. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 88. Press the INITIATE pushbutton switch and observe:
 - a. Segment B of the diagnostic tape lads into memory.
 - b. PRGM HALT indicator illuminates at the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00000645.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE CONTENTS OF MEMORY PAGE ZERO INTO MEMORY PAGE 2

- 89. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 90. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 91. Set the WSR toggle switches to 00000664.
- 92. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00000664.
- 93. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 94. Press the INITIATE pushbutton switch and observe:
 - a. PRGM HALT indicator Illuminates.
 - b. BUS INDICATOR displays a reading of 00000702.

THE FOLLOWING PROCEDURES EXECUTE SEGMENT B TO TEST PAGE ZERO

- 95. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 96. Set the WSR toggle switches to 00242000.

- 97. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator is illuminated.
- 98. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00242000.
- 99. Set the WSR toggle switches to all 0's.
- 100. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 101. Press the INITIATE pushbutton switch and observe the following after approximately 25 seconds:
 - a. PRGM HALT indicator illuminates.
 - b. BUS INDICATOR displays a reading of 00242507.
 - c. END MEM B message is generated on the page printer.

Section III. TROUBLESHOOTING CHART

Probable cause	Corrective action
Faulty DLP assembly A11 (Memory data register stage failure).	Replace DLP assembly A11; then repeat test.
Faulty DLX assembly A12 (inhibit select switch or sense amplifier	Replace DLX assembly A12; then repeat test.
Faulty DLX assembly A13 (inhabit select switch or sense amplifier	Replace DLX assembly A13; then repeat test.
Faulty DLP assembly A11 (inhabit select switch or sense amplifier	Replace DLP assembly A11; then repeat test.
Faulty DLP assembly A11 (memory data register parity bit stage failure).	Replace DLP assembly A11; then repeat test.
Faulty DLX assembly A12.	Replace DLX assembly A12; then repeat test.
Faulty DLX assembly A13.	Replace DLX assembly A13; then repeat test.
Faulty DLP assembly A11.	Replace DLP assembly A11; then repeat test.
	 Probable cause Faulty DLP assembly A11 (Memory data register stage failure). Faulty DLX assembly A12 (inhibit select switch or sense amplifier Faulty DLX assembly A13 (inhabit select switch or sense amplifier Faulty DLP assembly A11 (inhabit select switch or sense amplifier Faulty DLP assembly A11 (memory data register parity bit stage failure). Faulty DLX assembly A12. Faulty DLX assembly A13. Faulty DLY assembly A13.

Section IV. UNSCHEDULED INTERRUPTS

If the diagnostic program halts at a BUS INDICATOR reading of 00002747, the diagnostic program is attempting to generate an output to the local page printer but the Character Ready is too long.

a. Press the system status panel RESET pushbutton switch and restart the diagnostic program at step 42, Section II.

b. If the diagnostic program continues to halt at address 00002747, replace the three (3) sync circuit cards associated with the local page printer.

If the diagnostic program halts at a BUS INDICATOR reading of 00003026, the diagnostic program has timed out when using the local page printer.

a. Press the system status panel RESET pushbutton switch and restart the diagnostic program at step 62, Section II.

b. If the program continues to halt at address 00003026, replace the three (3) sync circuit cards associated with the local page printer.

Section V. TROUBLESHOOTING TRANSIENT MALFUNCTIONS

- 1. Execute steps 1 through 41 of the Diagnostic Program, Section II.
- 2. Set the WSR toggle switches 00 and 06 to a 1.
- 3. Set the memory cards H-L switch to position H.
- 4. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 5. Press the INITIATE pushbutton switch and observe that the program continues to loop on the complete diagnostic program without stopping.
- 6. If no errors are detected after approximately 10 minutes, reset the WSR06 bit and observe:
 - a. PRGM HALT indicator illuminates.
 - b. BUS INDICATOR displays a reading of 00002507.
- 7. Select any other option (Section VI) or group of options and press the INITIATE pushbutton switch.
- 8. Reset all WSR bits, except WSR00, to stop the testing cycle.
- 9. Set both memory card H-L switches to L.
- 10. Set WSR toggle switches 00 and 06 to a 1.
- 11. Press the INITIATE pushbutton switch and observe that the same indications obtained in step 6 above are obtained.
- 12. Execute steps 42 through 61 of the Diagnostic Program, Section II.
- 13. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 14. Set WSR0 and WSR06 to a 1.
- 15. Press the INITIATE pushbutton switch and observe that the program continues to loop on the complete diagnostic program without stopping.
- 16. If no errors are detected after approximately 10 minutes, reset WSR06 and observe that: *a.* PRGM HALT indicator illuminates.
 - b. BUS INDICATOR displays a reading of 00002507.
- 17. Set both memory card H-L switches to the normal (center) position.

Section VI. PROGRAM OPTIONS

Option 1 = WSR0 and WSR1 set: (Inhibit Printer)

In this mode, all printing on the teletype is bypassed. Whatever information that would normally be printed as a failure report will have to be determined by reading the memory locations that contain information.

A data parity error (DPE) will halt the diagnostic program at address location 2612 and the accumulator has the exact address at which the processor interrupt occurred. A write/read error will not produce an error indication.

Option 2 = WSR0 and WSR2 set: (Halt on Error)

This mode is used to discover errors as they occur. Whenever an error does occur, the pattern number, address, and word read is placed in the A and Q registers, respectively, and the program halts. A write/read error will halt the diagnostic program at address location 2571. The A register bits 06 through 23 will equal the location read that failed and the A register bits 0 through 02 will equal the pattern number. The Q register will equal incorrect data read from memory.

Option 3 = WSR0 and WSR3 set: (Loop on Individual Pattern)

This mode is used to keep the diagnostic program operating within a specific pattern. The program will halt at address location 2153 if the incorrect pattern is set into the WSR toggle switches. Select the correct pattern number from the chart below and press the INITIATE pushbutton switch to loop.

Pattern No.	Description	WSR12	WSR13	WSR14
0	All zeros (0's) for fluxchange	0	0	0
1	All ones (1's) for non-fluxhange	0	0	1
2	Write address into memory	0	1	0
3	Write address complement into memory	0	1	1
4	Worst case pattern for sensors	1	0	0

Option 4 = WSR0 and WSR4 set: (Loop on Particular Page)

The mode is used to keep the diagnostic program operating within a specific page. Unless option 3 above is selected, the diagnostic program will loop on all patterns. The program will halt at address location 2127 if an incorrect page has been selected for the particular segment of the program. Select the correct page number from the chart below and press the INITIATE pushbutton switch to loop.

Legal page	Page	WSR10	WSR11
Segment B only	0	0	0
Segment A and B	1	0	1
Segment A only	2	1	0

Option 5 = WSR0 and WSR5 set: (Halt at End of Pattern Test)

The diagnostic program will halt at address location 2423. The address will be stored in the A register and the pattern number will be stored in the Q register. Press the NORMAL HALT pushbutton switch and set the REGISTER SELECT rotary switch to the desired register position. The BUS INDICATOR will display either the address or pattern number as selected.

Option 6 = WSR0 and WSR6 set: (Loop on Entire Test)

This mode is used to loop this entire diagnostic program. Segment A will loop on page 1 and 2 using all test pattern. Segment B will loop on page zero using all test patterns. *Option* 7 = *WSR0* and *WSR7* set: (Store Memory Test Pattern with 10 Writes per Location)

Location 00003107 can be altered to either increase or decrease the number of write instructions. The number of writes should be entered using the octal equivalent.

Option 8 = WSR0 and WSR23 set: (Restore Contents of Memory Page following Segment B test)

This option must be executed any time the user transfers from Segment B back to Segment A of the diagnostic program. Set the PEX to 664 in order to restore the loader program to page zero and then read in Segment A into memory.



Figure 2 (1). Memory Logic Data Flow Diagram (Sheet 1 of 7).



Figure 2 (2). Memory Logic Data Flow Diagram (Sheet 2 of 7).



Figure 2 (3). Memory Logic Data Flow Diagram (Sheet 3 of 7).



Figure 2 (4). Memory Logic Data Flow Diagram (Sheet 4 of 7).



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Figure 2 (5). Memory Logic Data Flow Diagram (Sheet 5 of 7).

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Figure 2 (6). Memory Logic Data Flow Diagram (Sheet 6 of 7).



Figure 2 (7). Memory Logic Data Flow Diagram (Sheet 7 of 7).

EXHIBIT D

COMMON CONTROL SYNCHRONIZER DIAGNOSTIC PROGRAM

Section I. GENERAL

The Common Control Synchronizer diagnostic program is used whenever memory-to-memory, functional assignment control panel, or peripheral device data transfer problems are encountered. The diagnostic procedures check the central processor-synchronizer interface and data handling capability. Successful completion of the diagnostic program verifies synchronizer control logic, establishes the existence and correct operational ability of each synchronizer to receive and store selected data patterns, and checks the buffer register and data steering circuitry of the AN/TTC-38(V).

Error printouts generated during the execution of the diagnostic program can be used to minimize the search for malfunctioning logic circuits. After executing the corrective action, the diagnostic program should be repeated to verify that the AN/TTC-38(V) system is now functional.

Section II. DIAGNOSTIC PROGRAM

THE FOLLOWING PROCEDURES ARE USED TO CONVERT THE OPERATIONAL PRELOADER PROGRAM TO THE OFF-LINE DIAGNOSTIC PRELOADER PROGRAM

- 1. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 2. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 3. Set the WSR toggle switches to 00277750.
- 4. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 5. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A.
- 6. Set the WSR toggle switches to 5513774.
- 7. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified on the on-line program preloader instruction entries chart below. If the entries do not agree, or a absent, the on-line program preloader instructions must be loaded into memory before proceeding. If the entries appearing in parenthesis on the chart are already loaded into memory, proceed to step 42 below.
- 8. Set the MEMORY guarded switch to the UNPROTECTED position.
- 9. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator Illuminates.
- 10. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 11. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 12. Verify that the CLOCK OPERATE CONTROL rotary switch is in the CONT position.
- 13. Press the CLEAR pushbutton switch.
- 14. Set the WSR toggle switches to 00277750.
- 15. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 16. Set the OPERATIONAL CONTROL rotary switch to STORE SEQL and the REGISTER SELECT to MEM.

- 17. Set the WSR toggle switches to the instruction entries listed in the on-line preloader instruction chart and press the INITIATE pushbutton switch after each setting. Observe that the BUS INDICATOR displays the entered instruction.
- 18. Press NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator lights.
- 19. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 20. Set the WSR toggle switches to 00277750.
- 21. Press the INITIATE pushbutton switch and observe that BUS INDICATOR displays the address listed.
- 22. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A.
- 23. Set the WSR toggle switches to 55137754.
- 24. Press INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified on the chart.

NOTE

The following procedures will correct an erroneous address entered from the chart of specified addresses and instructions.

- a. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- b. Set the ASR toggle switches to the correct address.
- c. Press INITIATE pushbutton switch and observe that the BUS INDICATOR displays the correct address.
- d. Set the WSR toggle switches to the correct instruction number.
- e. Set the OPERATIONAL CONTROL rotary switch to STORE.
- f. Press INITIATE pushbutton switch and observe BUS INDICATOR displays the correct instruction.
- g. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- h. Press INITIATE pushbutton switch and verify that the BUS INDICATOR displays the correct instruction.

Preloader Instructions Chart

Address	Instruction
00277750	01077761
00277751	00002404
00277752	05200377
00277753	24077755
00277754	22077750
00277755	7010000
00277756	7000001
00277767	01077760
00277760	00002400
00277761	02200040
00277762	24077757
00277763	01077764
00277764	00002404
00277765	34000020
00277766	35000010
00277767	72000001
00277770	7400003
00277771	22077757
00277772	62601776 (62500476)
00277773	72100001
00277774	74100107 (74100235
00277776	22077756
00277776	0000000

- 25. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 26. Set the MEMORY guarded switch to the UNPROTECTED position.
- 27. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- 28. Set the ASR toggle switches to 277772.
- 29. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62501776.
- 30. Set the WSR toggle switches to 62500476.
- 31. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 32. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62500476.
- 33. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 34. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62500476.
- 35. Set the ASR toggle switches to 277774.
- 36. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100107.
- 37. Set the WSR toggle switches to 74100235.
- 38. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 39. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100235.
- 40. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 41. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100235.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE OFF-LINE DIAGNOSTIC LOADER PROGRAM INTO MEMORY

- 42. Load the off-line diagnostic loader tape (SM-D-752126) on the paper tape reader.
- 43. Set the paper tape reader MODE SELECT toggle switch to STRIP and the PWR switch to ON.
- 44. Set the system status panel RESET SELECT TAPE READER toggle switch to ON.
- 45. Press the system status panel RESET pushbutton switch several times and observe that the loader tape moves.
- 46. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 47. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 48. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 49. Set the WSR toggle switches to 00277780.
- 50. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 51. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 52. Set the RUN/ONE INSTR toggle switch to RUN.
- 53. Press the INITIATE pushbutton switch and observe that:
 - a. Off-line diagnostic loader tape strip loads into memory.
 - b. PRGM HALT indicator illuminates at the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00277777.
- 54. Rewind the loader tape by setting the system status panel TAPE READER REWIND toggle switch to ON.
- 55. Set the PARITY ERROR HALT toggle switch to OFF.
- 56. Set the CLOCK OPERATE CONTROL rotary switch to CONT.
- 57. Set the ADV-RPT toggle switch to ADV.

- 58. Set the REAL TIME CLOCK guarded switch to the ENABLE position.
- 59. Set the MEMORY guarded switch to the PROTECTED position.
- 60. Set the CONTROL TRANSFER toggle switch to DISABLE.
- 61. Set the printer motor control BYPASS toggle switch to BYPASS.

THE FOLLOWING PROCEDURES LOAD THE DIAGNOSTIC PROGRAM INTO MEMORY

- 62. Load the common Control Sync (SM-D-751720) and Remote Device Sync (SM-D-751721) Diagnostic Program tapes on the paper tape reader.
- 63. Set the paper tape reader MODE SELECT toggle switch to REEL and the PWR switch to ON.
- 64. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates and the PRGM HALT indicator extinguishes.
- 65. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 66. Set the WSR toggle switches to 0000500.
- 67. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 0000500.
- 68. Press the system status panel RESET pushbutton switch several times and observe that the diagnostic tape moves.
- 69. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 70. Press the INITIATE pushbutton switch and observe:
 - a. Diagnostic program tape loads into memory.
 - b. PRGM HALT indicator illuminates at the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00000631.
- 71. Rewind the diagnostic program tape by setting the system status panel TAPE READER REWIND toggle switch to ON.
- 72. Remove the diagnostic tape reel from the paper tape reader because it will cause an error printout when the diagnostic program is executed.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE STARTING ADDRESS INTO THE PROGRAM COUNTER

- 73. Set the REGISTER SELECT rotary switch to PEX.
- 74. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 75. Press the CLEAR pushbutton switch.
- 76. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 77. Set the WSR toggle switches to 00020000.
- 78. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00020000.
- 79. Set the system status panel RESET SELECT LOCAL PRINTER toggle switch to ON and press the RESET pushbutton switch.
- 80. Set the WSR toggle switches to all 0's.

THE FOLLOWING PROCEDURES ARE USED TO EXECUTE THE DIAGNOSTIC ROUTINE

- 81. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 82. Set all system status pane RESET SELECT toggle switches to ON position and press the RESET pushbutton several times.
- 83. Return all system status panel RESET SELECT toggle switches to the OFF position.
- 84. Press the INITIATE pushbutton switch and observe that:
 - a. CS TEST message is generated on the page printer.
 - b. PRGM HALT indicator illuminates.
 - c. BUS INDICATOR displays a reading of 00023212.
 - d. END CS TEST message is generated on the page printer.

- 85. Visually inspect for a flashing FUNCTION CODE indicator lamp on the Functional Assignment Control Panel (FACP).
- 86. Press the FACP CLEAR pushbutton switch and observe that the FUNCTION CODE indicator is extinguished.

Section III. POSSIBLE PROGRAM HALTS

Halt Address	Remarks
00020455	More than 8 unscheduled interrupts occurred while executing the diagnostic program. Proceed to the Bootstrap Diagnostic Program test the CPS logic.
00021047	The BUSY bit associated with the local page printer will not reset. Restart the program at step 73, Section II.

Section IV. PROCEDURES TO EXECUTE A FAILING INPUT/OUTPUT INSTRUCTION BY THE MAINTENANCE CONTROL PANEL

- 1. Utilize any available error messages to determine the input/output instruction that is failing.
- 2. Set the appropriate system status panel RESET SELECT toggle switch and press the RESET pushbutton several time.

3. For any write instruction, the accumulator must be loaded with the data as follows:

- a. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- b. Set the REGISTER SELECT rotary switch to position A.
- Set the WSR toggle switch bits 16 through 23 to the desired data.
- c. Set the WSR toggle switch bits 16 through 23 to the desired data.
 d. Press INITIATE pushbutton switch and observe that the BUS INDICATOR displays the WSR toggle switch settings.
- Execute the failing input/output instruction as follows: 4.
 - a. Set the REGISTER SELECT rotary switch to position A.
 - b. Set the WSR toggle switches to 0120CCDD; where,
 - CC = Device
 - 00 = RPT Remote Page Printer
 - 04 = PTP Punch
 - 10 = LPP Local Page Printer
 - 14 = EXR Spare TTY receiver
 - 20 = EXT Spare TTY transmitter
 - 24 = PTR Paper Tape Reader
 - 30 = MTM Memory to Memory
 - 34 = TYR Remote TTY receiver
 - 40 = TYT Remote TTY transmitter
 - 44 = FACP Functional Assignment Control Panel
 - DD = Instruction
 - 00 = Read Status
 - 01 = Clear Out Reset Busy Bit
 - 04 = Read data and Reset CHRRDY
 - 10 = Write Status and Set CHRRDY
 - 14 = Write Data and Set CHRRDY
 - 20 = Read Status and Set Busy Bit.
 - c. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR.
 - d. Set the RUN/ONE INSTR toggle switch to RUN.
 - e. Press the INITIATE pushbutton switch and observe that the ACTIVE indicator illuminates.
 - Use the logic drawings in TM 11-5805-628-34-6 and an oscilloscope to troubleshoot the fault. f

5. The following represents status that will appear in the accumulator when executing a status instruction:

Remarks
TRE - Timing Read Error
VA - Device Alarm
BB-Busy Bit
CHAR. LOST - Character Lost.

Section V. SYNCHRONIZER ERROR PRINTOUTS

	Malfunction	Probable cause	Corrective action
1.	PIOCS 01-XX where XX is two-digit	Processor timeout fault.	Use other processor to control AN/TTC-
2.	PIOCS02-01	Data read from paper tape reader (PTR) synchronizer buffer differs from data written into it by test program.	Replace following cards in sequence. Rerun test after each replacement (1) A16A103 (2) A16A102 (3) A16A101
3.	PIOS03-XX-YYY where XX is 01 through 12, XX and YYY both identify faulty synchronizer. For XX = 77 see 10 below:	Data read from synchronizer YYY buffer differs from data written into it by test program.	Replace following synchronizer YYY cards in sequence. Rerun test after replacement. (1) MOS 3
XX 01 02 03 04 05 06	YY RPP (remote page printer) PTP (paper tape punch) LPP (local page printer) EXR (extra receive) EXT (extra transmit) PTR (paper tape reader)		(2) MOS 2 (3) MOS 1
07 10 11	MTM (memory to memory) TYR (teletype receive) TYT (teletype transmit)		
12 4.	PIOCS04-XXYY where XX is 01 through 12, refer to 3 above, for XX and YYY, for XX = 77 see	Busy bit (BB) failed to set in synchronizer YYY.	Replace synchronizer YYY MOS 2 card. Rerun test.
5.	PIOCS05-XX-YY where XX is 01 through 12, refer to 3 above for XX and YYY, for XX = 77 see 10 below.	Busy bit (BB) failed to reset in synchronizer YYY.	Replace synchronizer YYY MOS 2 card. Rerun test.
6.	PISC06-XX-YYY where XX is 01 through 12, refer to 3 above for XX and YYY, for XX = 77 see 10 below.	Character ready (CH RDY) failed to set in synchronizer YYY.	Replace synchronizer YYY MOS 2 card. Rerun test.
7.	PIOCS07-XX-YY where XX is 01 01 through 12, refer to 3 above for XX and YYY, for XX = 77 see 10 below.	Character ready (CH RDY) failed to reset in synchronizer YYY.	Replace synchronizer YYY MOS 2 card, Rerun test.
8.	PIOCS08-XX-YYY-DO = XXX where XX is 01 through 04 XX and XXX identify data sent to synchronizer buffer by test program. For XX = 77 see 10	Data read from synchronizer YYY buffer differs from data written into it. Data written as XXX.	Replace the following synchronizer YYY cards in sequence. Rerun test after each replacement. (1) MOS 3 (2) MOS 2 (3) MOS 1
хх	XXX		

^{01 200} 02 325

	Malfunction	Probable cause	Corrective action
03	352		
04	277		
	Refer to 3 above for YYY.		
9.	Piocsop-XX-FAC where XX is a two-digit number.	Error indicator malfunction in FACP.	Use other processor to control AN/TTC-38(V).
10.	PIOCS XX ^T MO AT LOC XXXXX PGE 00 PIOCS XX-77-YYY.	Synchronizer YYY did not respond in time when executing instruction at XXXXX during test XX.	Replace synchronizer YYY MOS 2 card. Rerun test.

EXHIBIT E

REMOTE DEVICES DIAGNOSTIC PROGRAM

Section I. GENERAL

- The Remote Devices diagnostic program is used whenever data transfer problems are encountered with the operation of the remote page printer, remote teletypewriter, or spare remote teletypewriter. Successful completion of the program verifies the operational capabilities of the synchronizers, modern lines, and devices for the AN/TTC-38(V) configuration selected.
- Printing errors which may be observed while running the tests and ASCII and Baudot code printouts are included. A remote devices replacement table identifying driver and receiver cards and the modem modules are also included. After executing the suggested corrective action, the diagnostic procedures should be repeated to verify the system is operating properly.

Section II. DIAGNOSTIC PROGRAM

THE FOLLOWING PROCEDURES ARE USED TO CONVERT THE OPERATIONAL PRELOADER PROGRAM TO THE OFF-LINE DIAGNOSTIC PRELOADER PROGRAM

- 1. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 2. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 2.1. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 3. Set the WSR toggle switches to 00277750.
- 4. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 5. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A.
- 6. Set the WSR toggle switches to 55137754.
- 7. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified on the on-line program preloader instruction entries chart below. If the entries do not agree, or are absent, the on-line program preloader instructions must be loaded into memory before proceeding. If the entries appearing in parenthesis on the chart are already loaded into memory, proceed to step 42 below.
- 8. Set the MEMORY guarded switch to the UNPROTECTED position.
- 9. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT Indicator illuminates.
- 10. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 11. Verify that the RUN/ONE INSTR toggle switch is set to ONE INSTR.
- 12. Verify that the CLOCK OPERATE CONTROL rotary switch is in the CONT position.
- 13. Press the CLEAR pushbutton switch.
- 14. Set the WSR toggle switches to 00277750.
- 15. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 16. Set the OPERATIONAL CONTROL rotary switch to STORE SEQL and the REGISTER SELECT to MEM.

- 17. Set the WSR toggle switches to the instruction entries listed in the on-line preloader instruction chart and press the INITIATE pushbutton switch after each setting. Observe that the BUS INDICATOR displays the entered instruction.
- 18. Press NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator lights.
- 19. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 20. Set the WSR toggle switches to 00277750.
- 21. Press the INITIATE pushbutton switch and observe that BUS INDICATOR displays the address listed.

Preloader Instructions Chart

Instruction
01077751
00002404
06200377
24077755
22077750
70100000
7000001
01077760
00002400
02000040
24077764
01077764
00002404
34000020
36000010
7200001
7400003
22077757
62501776 (62500476)
72100001
74100107 (4100235)
22077756
0000000

- 22. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A.
- 23. Set the WSR toggle switches to 561377654.
- 24. Press INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified on the chat.

NOTE

The following procedures will correct an erroneous address entered from the chart of specified addresses and instructions.

- a. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- b. Set the ASR toggle switches to the correct address.
- c. Press INITIATE pushbutton switch and observe that the BUS INDICATOR displays the correct address.
- *d.* Set the WSR toggle switches the correct instruction number.
- e. Set the OPERATIONAL CONTROL rotary switch to STORE.
- *f.* Press INITIATE pushbutton switch and observe BUS INDICATOR displays the correct instruction.
- g. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- h. Press INITIATE pushbutton switch and verify that the BUS INDICATOR displays the correct instruction.

- 25. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 26. Set the MEMORY guarded switch to the UNPROTECTED position.
- 27. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- 28. Set the ASR toggle switches to 277772.
- 29. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62501776.
- 30. Set the WSR toggle switches to 62500476.
- 31. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 32. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62500476.
- 33. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 34. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62500476.
- 35. Set the ASR toggle switches to 277774.
- 36. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100107.
- 37. Set the WSR toggle switches to 74100235.
- 38. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 39. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100235.
- 40. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 41. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100235.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE OFF-LINE DIAGNOSTIC LOADER PROGRAM INTO MEMORY

- 42. Load the off-line diagnostic loader tape (SM-D-752126) on the paper tape reader.
- 43. Set the paper tape reader MODE SELECT toggle switch to STRIP and the PWR switch to ON.
- 44. Set the system status panel RESET SELECT TAPE READER toggle switch to ON.
- 45. Press the system status panel RESET pushbutton switch several times and observe that the loader tape moves.
- 46. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 47. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 48. Set the RUN/ONE INSTR toggle to ONE INSTR.
- 49. Set the WSR toggle switches to 00277750.
- 50. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 51. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 52. Set the RUN/ONE INSTR toggle switch to RUN.
- 53. Press the INITIATE pushbutton switch and observe that:
 - a. Off-line diagnostic loader tape strip loads into memory.
 - *b.* PRGM HALT indicator illuminates the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00277777.
- 54. Rewind the loader tape by setting the system status panel TAPE READER REWIND toggle switch to ON.
- 55. Set the PARITY ERROR HALT toggle switch to OFF.
- 56. Set the CLOCK OPERATE CONTROL rotary switch to CONT.
- 57. Set the ADV-RPT toggle switch to ADV.
- 58. Set the REAL TIME CLOCK guarded switch to the ENABLE position.
- 59. Set the REGISTER SELECT rotary switch to PEX.
- 60. Set the CONTROL TRANSFER toggle switch to DISABLE.

- 61. Set the printer motor control BYPASS toggle switch to BYPASS.
- 62. Set the MEMORY guarded switch to the PROTECTED position.
- 63. Set both modem L-B NOR-LOC rotary switches to NOR.

THE FOLLOWING PROCEDURES LOAD THE DIAGNOSTIC PROGRAM INTO MEMORY

64. Load the Common Control Sync (SM-D-751720) and Remote Devices Sync (SM-D-751721) Diagnostic Program tapes on the paper tape reader.

NOTE

The one segment of Common Control Sync diagnostic program must be loaded into memory prior to loading the one segment Remote Devices Sync diagnostic tape.

- 65. Set the paper tape reader MODE SELECT toggle switch to REEL and the PWR switch to ON.
- 66. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates and the PRGM HALT Indicator extinguishes.
- 67. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 68. Set the WSR toggle switches to 00000500.
- 69. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00000500.
- 70. Press the system status panel RESET pushbutton switch several times and observe that the diagnostic tape moves.
- 71. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 72. Press the INITIATE pushbutton switch and observe that:
 - a. Diagnostic program tape loads into memory.
 - b. PRGM HALT indicator illuminates a the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00000631.
- 73. Press the INITIATE pushbutton switch a second time to read-in the Remote Devices Sync diagnostic segment into memory. The same indications observed in step 72 above should be observed.
- 74. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- 74.1 Set the ASR toggle switches to 32642.
- 74.2. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 74.3. Set the WSR toggle switches to 00000037.
- 74.4. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00000040.
- 74.5. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 74.6. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00000037.
- 74.7. Set the REGISTER SELECT rotary switch to PEX.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE STARTING ADDRESS INTO MEMORY

- 75. Press the NORMAL HALT pushbutton switch and observe the PRCS HALT indicator illuminates.
- 75.1. Press the CLEAR pushbutton switch.
- 76. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 77. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 78. Set the WSR toggle switches to 00025000.
- 79. Press the INITIATE pushbutton switch and observe the BUS INDICATOR displays a reading of 00025000.

THE FOLLOWING PROCEDURES ARE USED TO TEST THE LOCAL PAGE PRINTER

- 80. Observe that the page printer has been marked out-of-service:
 - a. Set the ON-LINE processor function code to 17.
 - b. Set ASR bit 09 and ASR bit 21 to a 1.
 - *c.* Press the READ pushbutton switch.
- 81. Set the WSR toggle switches to 70000200.
- 82. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 83. Set the RUN/ONE INSTR toggle switch to RUN.
- 84. Press the INITIATE pushbutton switch and observe that:
 - a. Complete alphabet message is generated on page printer.
 - b. BUS INDICATOR displays a reading of 00027576.

NOTE

If the diagnostic program halts at any address other than 00027576, refer to the HALT TABLE below and replace the specified cards in order. Repeat the procedures in steps 80 through 84 above after each replacement.

BUS INDICATOR reading

Suggested Replacements

00026410	A16A133 (MOS 2)
00026451	A16A133 (MOS 2)
00026502	A16A133 (MOS 2)
00026532	A16A133 (MOS 2)
00026612	A16A133 (MOS 2)
00026652	A16A133 (MOS 2)
00026704	A16A133 (MOS 2)
00026743	A16A133 (MOS 2)
00027017	A16A134, A16A133, A16A132, in sequence
00027055	A16A134, A16A133, A16A132, in sequence
00027105	A16A134, A16A133, A16A132, in sequence
00027245	A16A134 (MOS 3)
00027315	A16A134 (MOS 3)
00027352	A16A134 (MOS 3)
00027411	A16A134 (MOS 3)
00027505	A16A134 (MOS 3)
00027450	Verify REAL TIME CLOCK guarded switch is in ENABLE position. Verify
00025243	the setting of WSR toggle switches.
00025375	
00026262	Execute the bootstrap diagnostic program.
00025435	

85. Set the ON-LINE processor ASR bit 21 to 0 and ASR bit 20 to 1.

86. Press the READ pushbutton switch.

THE FOLLOWING PROCEDURES TEST THE REMOTE PAGE PRINTER WITH EITHER THE REMOTE TTY OR SPARE TTY

- 87. Set the ON-LINE processor ASR bits 07, 10, 13, and 21 to 1.
- 88. Press the READ pushbutton switch and observe that the following message is generated on the local page printer: DEV #0 out SVC
 - DEV #3 out SVC
 - DEV #6 out SVC
- 89. Set the WSR toggle switches to the following:
 - a. If the remote page printer code select is Baudot:
 - (1) Remote tty = 00020007
 - (2) Spare tty = 00020003

- b. If the remote page printer code select is ASCII:
 - (1) Remote tty = 00000007
 - (2) Spare tty = 0000003
- 90. Set the OPERATIONAL CONTROL rotary switch to CMPT and REGISTER SELECT to PEX.
- 91. Set the RUN/ONE INSTR toggle switch to RUN.
- 92. Press the INITIATE pushbutton switch and observe that:
 - a. DEVICE TEST message is generated on page printer (indicates program is running tests 01 through 04).
 - b. END TEST message is generated at completion of test 04.
 - c. BUS INDICATOR displays a reading of 00027576.
- 93. Observe that the following test message(s), depending on the classmarking, is generated on the remote page printer. A. ASCII Test Message

!'\$%&'()*+,-./0123456789:; =? ABCDEFGHIJKLMNOPQRSTUVWXYZ + ABCDEFGHIJKLMNOPQRSTUVWXYZ

ABCDEFGHIJKLMNOPQRSTUVWXYZ

B. BAUDOT Test Message

- 94. If the observed test message in step 80 above is inaccurate, replace cards A16A120, A16A119, and A16A118, in sequence, and repeat the procedures in steps 87 through 93 above after each replacement.
- 95. Place a vertical strap 4-wire patch cord on the common equipment panel between either the remote page printer (PTR) to the remote tty (TTY) or spare tty (SPTTY).

NOTE

Both devices must be in either the direct or modem configuration which can be determined by the position of the toggle switches at the rear of the system status panel.

- 96. Set the system status panel REMOTE PRINTER and TTY or SPARE TTY toggle switches to ON.
- 97. Press the RESET pushbutton switch several times.
- 98. Press the INITIATE pushbutton switch and observe:
 - a. Change ASCII/Baudot SW SYNC A message is generated on page printer.
 - b. BUS INDICATOR displays a reading of 00031217 (indicates test 05 through 09 have been completed).

THE FOLLOWING PROCEDURES TEST THE TIMING READ ERROR FLIP- FLOP

- 99. Set the remote page printer code select switch (located behind the system status panel) to BAUDOT and the remote tty to ACSII position.
- 100. Press the INITIATE pushbutton switch and observe:
 - a. CHANGE ASCII/BAUDOT SW SYNC MAYBE message generated on page printer.
 - b. BUS INDICATOR displays a reading 00031457 (indicates completion of test 10).
- 101. Set the remote tty or spare tty code select switch to agree with the remote page printer code select switch.
- 102. Press the INITIATE pushbutton switch and observe:
 - a. Test 12 BYPASSED and END TEST message generated on page printer.
 - b. BUS INDICATOR displays a reading of 00032252 (indicates completion of test 11).
- 103. Remove the patch cord inserted in step 95 above.
- 104. Set the ON-LINE processor ASR bit 21 to 0 and ASR bit 20 to 1.

THE FOLLOWING PROCEDURES TEST EITHER THE REMOTE TTY - SYNC A AND B OR SPARE TTY SYNC A AND B

- 105. Set the ON-LINE processor ASR bits 10, 13, 21 to 1.
- 106. Press the READ pushbutton switch.
- 107. Set the WSR toggle switches to the following:
 - a. If the remote device code select is BAUDOT:
 - Remote tty = 00021007
 - Spare tty = 00020403
 - b. If the remote device code select is ASCII:

Remote tty = 00001007

- Spare tty = 00000403
- 108. Set the OPERATION CONTROL rotary switch to CMPT and the REGISTER SELECT to PEX.
- 109. Set the RUN/ONE INSTR toggle switch to RUN.
- 110. Press INITIATE pushbutton switch and observe:
 - a. DEVICE TEST and END TEST message generated on page printer.
 - b. BUS INDICATOR displays a reading of 00027576.
- 111. Observe that the test message generated on the appropriate remote device is identical to that observed in step 93 above.
- 112. If the test message is inaccurate, replace the following cards, in sequence, and repeat the test:

Remote tty	Spare tty
A16A114	A16A139
A16A113	A16A128
A16A112	A16A127
A16A109	A16A126

- 113. Place a 2-wire patch cord on the COMMON EQUIPMENT PANEL between the send and receive pairs of the appropriate remote device quad connector. The setting of the mode select switch (rear of system status panel) determines if the direct or modem quad should be used.
- 114. Set the appropriate system status panel remote device toggle switch to ON.
- 115. Press the RESET pushbutton several times.
- 116. Press the INITIATE pushbutton switch and observe:
 - a. CHANGE ASCII/BAUDOT SW SYNC A message is generated on local page printer.
 - b. BUS INDICATOR displays a reading of 00031217 (Indicates tests 05 through 09 have been completed).
- 117. Press INITIATE pushbutton switch and observe:
 - a. CHANGE ASCII/BAUDOT SW SYNC A MAYBE message is generated on local page printer.
 - b. BUS INDICATOR displays a reading of 00031457 (Indicates test 10 had been completed).

NOTE

Test 10 cannot be executed correctly. Ignore any error messages related to test 10.

- 118. Press the INITIATE pushbutton switch and observe that:
 - a. PRCM HALT Indicator illuminates.
 - b. TEST 12 BYPASSED and END TEST messages are generated on the local page printer.
 - c. BUS INDICATOR displays a reading of 00032252.
- 119. Remove the patch cord inserted in step 113 above and restore the system to it original configuration.
- 120. Press the NORMAL HALT pushbutton switch.

- 121. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 122. Set the WSR toggle switches to 00032303.
- 123. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00032303.
- 124. Set the WSR toggle switches to the following:
 - a. If the remote device code select is BAUDOT:
 - Remote tty = 00061007
 - Spare tty = 00060403 b. If the remote device code select is ASCII:
 - If the remote device code select is ASC Remote tty = 00041007
 - Remote try = 0004100Spare try = 00040403
- 125. Notify the remote device operator that a typing test is to begin.
- 126. Press the INITIATE pushbutton.
- 127. Observe that approximately 3 minutes after the last test character has been received:
 - a. PGRM HALT indicator illuminates.
 - b. END TEST message is generated on page printer.
 - c. BUS INDICATOR displays a reading of 00032252.
- 128. Set the ON-LINE processor function code to 17 and mark the appropriate remote devices in-service:
 - ASR10 = 1 Spare tty
 - ASR13 = 1 Remote tty
 - ASR20 = 1 In-service
- 129. Press the READ pushbutton switch.

Section III. PROCEDURES TO MARK REMOTE DEVICES OUT-OF-SERVICE

- 1. Set the function code to 17.
- 2. Set the ASR toggle switches to 0's.
- 3. Select the device to be marked out-of-service:
 - 07 = remote page printer
 - 08 = tape punch
 - 09 = page printer
 - 10 = spare tty
 - 11= tape reader
 - 12 = memory-to-memory channel
 - 13 = remoter tty
 - 14 = FACP
- 4. Set ASR toggle switch bit 21 to a 1.
- 5. Press the READ pushbutton switch.

Section IV. ASCII AND BAUDOT CODE PRINTOUTS

XXX	<u>ASCII</u>	Baudot Key	XXX	ASCII	XXX	ASCII	XXX	ASCII
001	NUL	А	047	+	116	М	163	Р
002	SOH	В	050		117	Ν	164	Q
003	STX	С	051	(120	0	165	R
004	ETX	D	062)	121	Р	167	S
005	EOT	E	053	*	122	Q	170	Т
006	ENQ	F	054	+	123	R	171	U
007	ACK	G	055	3	124	S	172	V
010	BEL	Н	056	-	125	Т	173	W
011	BS	I	057	•	126	U	174	Х
012	HT	J	060	/	127	V	175	Y
013	LF	К	061	0	130	W	176	Z
014	VT	L	062	1	131	Х	177	(
015	FF	М	063	2	132	Y	200	ì
016	CR	Ν	064	3	133	Z	201)
017	SO	0	065	4	134	(202	
020	S	Р	066	5	135	1	203	DEL
021	DLE	Q	067	6	136)		
022	DC1	R	070	7	137			
023	DC2	S	071	8	140	-		
024	DC3	Т	072	9	141			
025	DC4	W	073	Ø	142	а		
026	NAK	V	074		143	b		
027	SYN	W	075)	144	С		
030	ETB	Х	076	=	145	d		
031	CAN	Y	077	3	146	е		
032	EM	Z	100		147	F		
038	UB	LETTERS SHIFT	101	•	150	CR		
064	ESC	FIGURES SHIFT	102	А	151	LF		
035	FS	SPACE	103	В	152	G		
086	GS	CARRIAGE RETURN	104	С	153	Н		
037	RS	LINE FEED	105	D	154			
040	US		106	E	155	J		
041	SP		107	F	156	K		
042	-		110	G	157	L		
043			111	Н	160	М		
044	=		112	Ι	161	Ν		
046	\$		113	J	162	0		
046	(114	K				
			115	L				

Section V. REMOTE DEVICES REPLACEMENT TABLE

			Modem
Synchronizer	Driver cards	Receiver cards	modules
TYR		A16A109, A16A177, A16A116	A13A1
TYT	A16A109	•	A13A2
RPP	A16A109	•	A13A3
EXT	A16A126	•	A13A4
EXR	•	A16A126, A16A117, A16A116	A13A5
LPP	A16A136	•	
PTP	A16A141	•	
PTR	•	A16W116, A16A117, A16A115	

Section VI. ERROR PRINTOUT MESSAGES

	Printout	Probable cause	Corrective action
1.	IODVA- <u>XX-XXX</u> where $\underline{XX} = 01$ or 02 and XXX = 001 or 002.	Status register filed.	Replace MOS2 card synchronizer A. Repeat test.
2.	IODVA-XX AT LOC \underline{XXXXX} PGE 00 IODVA XX-077 where $\underline{XX} =$ 01, 02 or 03 and \underline{XXXXX} identifies an address in memory page 0.	Synchronizer A did not respond in time when executing instruction at <u>XXXXXX</u> .	Replace MOS2 card synchronizer A. Repeat test.
3.	IODVA-03-XXX where XXX is 000, 125, 252 or 377 and represents data sent to buffer register by test program.	Data read from synchronizer A buffer register differs from data written. Data written was XXX.	Replace following synchronizer A cards in sequence. Repeat test after each replacement. (1) MOS 3 (2) MOS 2 (3) MOS 1
4.	IODVA-04- <u>XXX</u> . With CODE SELECT switches set to ASCII XXX = 001 through 20 and identifies ASCII character which failed. With switches set to 75 BAUD <u>XXX</u> - 001 through 037 and identifies Baudot character which failed.	Data read from synchronizer A buffer register differs from data written. Data written is identified by <u>XXX</u> .	Replace MOS 3 synchronizer A.
5.	IODVA-04-775	Incorrect timing for full ASCII or BAUDOT table.	Replace following card in sequence. Repeat test after each replacement. (1) MOS 3 synchronizer A (2) A7A216
6.	IODVA-04-776	Incorrect timing for single character.	Replace following cards in sequence. Repeat test after replacement. (1) MOS 3 synchronizer A (2) A16A216
7.	IODVA-04-TMOAT LOC XXXXX PGE00 IODVA-04-777 where XXXXXX.identifies an address in memory page 0.	Synchronizer A did not respond in time when executing instruction at <u>XXXXXX</u> .	Replace MOS 2 card synchronizer A. Repeat test.
8.	IODVB- <u>XX-XXX</u> where $\underline{XX} = 05$ or 06 and XXX = 001 or 002.	Status register failed.	Replace MOS 2 card synchronizer B. Repeat test.
9.	IODVB-XX-TMO AT LOC XXXXXX PGE 00 IODVB-XX-077 where XX = 05, 06 or 07 and XXXXXX identifies an address in memory page 0.	Synchronizer B did not respond in time while executing instruction at <u>XXXXXX</u> .	Replace MOS 2 card synchronizer B. Repeat test.
10.	IODVB-07-XXX where XXX = 000, 126 252, or 377 and represents data sent to buffer register by test program.	Data read from synchronizer differs from data written. Data written was <u>XXX</u> .	Replace following synchronizer B cards in sequence. Repeat test after each replacement. (1) MOS 3 (2) MOS 2 (3) MOS 1

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Printout	Probable cause	Corrective action
11. IODVB-08- <u>XXX</u> where <u>XXX</u> -0001 or	Status register failed.	Replace MOS2 card synchronizer B.
12. IODVB-08-002 (1) Test 4 failed. (2) Test 4 did not fail.	Related to results of test 04. (1) Refer to test 4. (2) Interrupt failure.	Relate to results of test 04. (1) Perform corrective action required for test 4 failure (1 above.) (2) Replace following device B cards in sequence. Repeat test after each replacement. (a) MOS 3 (b) MOS 2 (c) Receiver (d) Modem
13. IODVB-08-TMO-AT LOC XXXXXX PGE00 where XXXXXX identifies an address in memory page 0.	Illegal interrupt.	Replace following synchronizer B cards in sequence. Repeat test after each replacement. (1) MOS 3 (2) MOS 2
14. IODVB-XX-TMD AT LOC XXXXXX PGE00 IODVB-XX-077 where where XX = 08, 09 or 10 and XXXXXX identifies an address in memory page 0	Synchronizer did not respond on time when executing instruction at location <u>XXXXXX</u> .	Replace following cards in sequence. Repeat test after each replacement. (1) MOS 2 synchronizer A (2) MOS 2 synchronizer B
 15. IODVB-09-001 (1) Test 4 failed. (2) Test 4 did not fail. 	Related to result of test 4. (1) Refer to test 4. (2) Character lost (CHLST) failed.	Related to result of test 4. (1) Perform corrective action required for test 4 failure. (2) Replace the following device B cards in sequence. Repeat after each replacement. (a) MOS3 (b) MOS2 (c) Receiver (d) Modem
16. IODVB-09-002	Status register failed.	Replace MOS2 card synchronizer B. Repeat test.
17. IODVB-01-001 (1) Test 4 failed.	Related to result of test 4. (1) Refer to test 4.	Related to result of test 4. (1) Perform corrective action required for test 4 failure. (2) Replace following device B cards in sequence. Repeat test after each replacement. (a) MOS3 (b) MOS2 (c) Receiver (d) Modem
18. IODVB-10-002	Status register failed.	Replace MOS2 card synchronizer B. Repeat test.
19. IODVB-11- <u>XXX</u> . With CODE SELECT switches set to ASCII <u>XXX</u> = 001 through 203 and identifies ASCII character which failed with the switches set to 75 BAUD <u>XXX</u> = 001 through 037 and identifies Baudot character which failed.	Related to result of test 4.	Related to result of test 4.
(1) Test 4 failed.	(1) Refer to test 4.	(1) Perform correction action required for test 4 failure.
(2) Test 4 did not fail.	(2) Data transfer failure.	(2) Replace following device B cards in sequence. Repeat test after each replacement.

- (a) MOS3
 (b) MOS2
 (c) Receiver
 (d) Modem
| Printout | Probable cause | Corrective action |
|--|---|--|
| 20. IODVB- <u>XX</u> -774 where <u>XX</u> = 11 or 12. | Status register failed. | Replace following cards in sequence.
Repeat test after each replacement.
(1) MOS2 synchronizer B
(2) MOS2 synchronizer A |
| 21. IODVB-11-776 | Timing error. | Replace following cards in sequence.
Repeat test after each replacement.
(1) MOS1 synchronizer B
(2) MOS3 synchronizer B
(3) A7A216
(4) MOS1 synchronizer A
(5) MOS 3 synchronizer A |
| 22. IODVB- <u>XX</u> -TMO AT LOC <u>XXXXXX</u>
PGE00 IODVB- <u>XX</u> -777 where
<u>XX</u> = 11 or 12. | Synchronizer did not respond in time
when executing instruction at
location <u>XXXXXX</u> . | Replace following cards in sequence.
Repeat test after each replacement.
(1) MOS2 synchronizer B
(2) MOS2 synchronizer A |

EXHIBIT F

FUNCTIONAL ASSIGNMENT CONTROL PANEL **DIAGNOSTIC PROGRAM**

Section I. GENERAL

The Functional Assignment Control Panel (FACP) diagnostic program is used to test the functions involved in the transmission of data and instructions from the Central Processor to the FACP and the verification of FACP generated

codes. The series of tests requires the interaction of manual depression of the pushbutton switches and the response of the diagnostic program to the FACP generated character codes.

Section II. DIAGNOSTIC PROGRAM

THE FOLLOWING PROCEDURES ARE USED TO CONVERT THE OPERATIONAL PRELOADER PROGRAM TO THE OFF-LINE DIAGNOSTIC PRELOADER PROGRAM

- 1. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT Indicator illuminates.
- 2. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PFX.
- 3. Set the WSR toggle switches to 00277750.
- 4. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 5. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A.
- 6. Set the WSR toggle switches to 55137754.
- 7. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified on the on-line program preloader instruction entries chart below. If the entries do not agree, or are absent, the on-line program preloader instructions must be loaded into memory before proceeding. If the entries appearing in parenthesis on the chart are already loaded into memory, proceed to step 42 below

Address	Instruction
00277750	01077751
00277751	00002404
00277752	05200377
00277753	24077755
00277754	22077750
00277755	70100000
00277756	7000001
00277757	01077760
00277760	00002400
00277761	02200040
00277762	24077757
00277763	01077764
00277764	00002404
00277765	34000020
00277766	35000010
00277767	72000001

Address	Instruction
00277770	74000003
00277771	220777757
00277772	62501776 (62500476)
00277773	72100001
00277774	74100107 (74100235)
00277775	22077756
00277776	0000000

- 8. Set the MEMORY guarded switch to the UNPROTECTED position.
- 9. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 10. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 11. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 12. Verify that the CLOCK OPERATE CONTROL rotary switch is in the CONT position.
- 13. Press the CLEAR pushbutton switch.
- 14. Set the WSR toggle switches to 00277750.
- 15. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 16. Set the OPERATIONAL CONTROL rotary switch to STORE SEQL and the REGISTER SELECT to MEM.
- 17. Set the WSR toggle switches to the instruction entries listed in the on-line preloader instruction chart and press the INITIATE pushbutton switch after each setting. Observe that the BUS INDICATOR displays the entered instruction.
- 18. Press NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator lights.
- 19. Set the OPERATIONAL CONTROL ROTARY SWITCH TO STORE and the REGISTER SELECT to PEX.
- 20. Set the WSR toggle switches to 00277750.
- 21. Press the INITIATE pushbutton switch and observe that BUS INDICATOR displays the address listed.
- 22. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A.
- 23. Set the WSR toggle switches to 55137754.
- 24. Press INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified on the chart.

NOTE

The following procedures will correct an erroneous address entered from the chart of specified addresses and instructions.

- a. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- b. Set the ASR toggle switches to the correct address.
- c. Press INITIATE pushbutton switch and observe that the BUS INDICATOR displays the correct address.
- d. Set the WSR toggle switches to the *correct instruction number*.
- e. Set the OPERATIONAL CONTROL rotary switch to STORE.
- f. Press INITIATE pushbutton switch and observe BUS INDICATOR displays the correct instruction.
- g. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- *h*. Press INITIATE pushbutton switch and verify that the BUS INDICATOR displays the correct instruction.
- 25. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 26. Set the MEMORY guarded switch to the UNPROTECTED position.
- 27. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.

- 28. Set the ASR toggle switches to 277772.
- 29. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62501776.
- 30. Set the WSR toggle switches to 63500476.
- 31. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 32. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62500476.
- 33. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 34. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62500476. 35. Set the ASR toggle switches to 277774.
- 36. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100107.
- 37. Set the WSR toggle switches to 74100235.
- 38. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 39. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100235.
- 40. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 41. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100235.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE OFF-LINE DIAGNOSTIC LOADER PROGRAM INTO MEMORY

- 42. Load the off-line diagnostic loader tape (SM-D-752126) on the paper tape reader.
- 43. Set the paper tape reader MODE SELECT toggle switch to STRIP and the PWR switch to ON.
- 44. Set the system status panel RESET SELECT TAPE READER toggle switch to ON.
- 45. Press the system status panel RESET pushbutton switch several times and observe that the loader tape moves.
- 46. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 47. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 48. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 49. Set the WSR toggle switches to 00277750.
- 50. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 51. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 52. Set the RUN/ONE INSTR toggle switch to RUN.
- 53. Press the INITIATE pushbutton switch and observe that:
 - a. Off-line diagnostic loader tape strip loads into memory.
 - b. PRGM HALT Indicator illuminates at the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00277777.
- 54. Rewind the loader tape by setting the system status panel TAPE READER REWIND toggle switch to ON.
- 55. Set the PARITY ERROR HALT toggle switch to OFF.
- 56. Set the CLOCK OPERATE CONTROL rotary switch to CONT.
- 57. Set the ADV-RPT toggle switch to ADV.
- 58. Set the REAL TIME CLOCK guarded switch to the DISABLE position and the MEMORY guarded switch to the PROTECTED position.
- 59. Set the REGISTER SELECT rotary switch to PEX.
- 60. Set the CONTROL TRANSFER toggle switch to DISABLE.
- 61. Set the printer motor control BYPASS toggle switch to BYPASS.

THE FOLLOWING PROCEDURES LOAD THE DIAGNOSTIC PROGRAM INTO MEMORY

62. Load the Paper Tape Reader/Punch (SM-D-751722) and FACP (SM-D-751719) diagnostic program tape on the paper tape reader.

NOTE

The two segment Paper Tape Reader/Punch diagnostic program must be loaded into memory prior to loading the one segment FACP diagnostic program.

- 63. Set the paper tape reader MODE SELECT toggle switch to REEL and the PWR switch to ON.
- 64. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates and the PRGM HALT indicator extinguishes.
- 65. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 66. Set the WSR toggle switches to 00000500.
- 67. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 0000050.
- 68. Press the system status pane RESET pushbutton switch several times and observe that the diagnostic tape moves.
- 69. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 70. Press the-INITIATE pushbutton switch and observe:
 - a. Diagnostic program tape loads into memory.
 - b. PRGM HALT indicator illuminates at the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00000631.
- 71. Press the INITIATE pushbutton for a total of three (3) times to read-in the FACP diagnostic program and observe that the same Indications obtained in step 70 above are obtained.
- 72. Rewind the diagnostic program tape by setting the system status panel TAPE READER REWIND toggle switch to ON.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE STARTING ADDRESS INTO THE PROGRAM COUNTER

- 73. Set the REGISTER SELECT rotary switch to PEX.
- 74. Press the NORMAL HALT pushbutton switch and observe the PRCS HALT indicator Illuminates.
- 75. Press the CLEAR pushbutton switch.
- 76. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 77. Set the WSR toggle switches to 00001000.
- 78. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00001000.
- 79. Set the system status panel RESET SELECT LOCAL PRINTER toggle switch to ON and press the RESET pushbutton switch.
- 80. Set the WSR toggle switches to all zeros.

THE FOLLOWING PROCEDURES ARE USED TO TEST THE INDICATOR LAMPS

- 81. Set the FACP LAMP TEST rotary switch to IND.
- 82. Press the FACP TEST pushbutton switch and observe that all Indicators illuminate.
- 83. Set the LAMP TEST rotary switch, in sequence, to DRO position 0 through 9 and press the TEST pushbutton switch. Observe that the selected digit is displayed on all readout indicators.
- 84. Set the LAMP TEST rotary switch to CLR.
- 85. Press the TEST pushbutton switch and observe that all readout Indicators extinguish.

THE FOLLOWING PROCEDURES ARE USED TO EXECUTE THE DIAGNOSTIC ROUTINES

- 86. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 87. Press the INITIATE pushbutton switch and observe that:
 - a. PRGM HALT indicator illuminates.
 - b. BUS INDICATOR displays a reading of 00010015.
 - c. FACP TEST message is generated on the local page printer.
- 88. Press the INITIATE pushbutton switch and observe that the FACP READY indicator lamp starts flashing (this indicates the end of tests 1 through 4).
- 89. Verify that all FACP indicators and digital readout indicators are off.
- 90. Press the FACP CONTINUE pushbutton switch and observe that the readout Indicator listed in the table below starts flashing and its DRO begins to fill in with the corresponding list of numbers.

Order	DRO and indicator	Displayed in DRO
1	TERMINAL NO	0101
2	TERMINAL TYPE	02
3	CLASS CODE	03
4	DIR NO	404
5	TRK GR NO	505
6	CONF	06
7	GR MIN COUNT	07
8	MODE II TERM NO	6086
9	SPCL CKT NO	09
10	PR NO	10
11	SL NO	11
12	STATUS	12
13	LINE GP NO	13
14	ALTN SL NO	14
15	FUNCTION CODE	5
16	RANK	6
17	PRI TRK GR NO	017
18	ALTN TRK GR NO	018
19	FIXED DIR NO/TRFC CNT	19019
20	FIXED DIR NO/TRFC CNT	02020
21	PR-SL-XXX/NNVXXXX	2121210
22	NARROW BAND-TOTAL	22
23	NARROW BAND-FO	23
24	NARROW BAND-FLASH	24
25	NARROW BAND-IMMED	25
26	NARROW BAND-PRI	26
27	WIDE BAND-TOTAL	27
28	WIDE BAND-PREC	28
29	OPERATORS-CALLS	29
30	OPERATORS-RECALLS	30
31	OPERATORS-INFO	31
32	OPERATORS-INTCP	32
33	TRUNK GR TRAFFIC-INCOM	33
34	TRUNK GR TRAFFIC-OUTGO	34
35	TRUNK GR TRAFFIC-RPMPT	35
36	TRUNK GR TRAFFIC-ATB	36
37	TRUNK GR TRAFFIC-LKOUT	37
38	READY	38
39	EERROR	39
40	STORE	40
41	READER TO TTY	41
42	READER TO SP TTY	42
43	READER TO PUNCH	43

91. Continue to press the CONTINUE pushbutton switch until all entries have been tested. At the completion of the table, observe that the READY indicator illuminates.

NOTE

The FACP readout indicators that do not have a DRO of its own will use the STATUS DRO.

92. Press one of the pushbutton switches listed in the table below and observe that the STATUS DRO displays the corresponding number.

NOTE

Any erroneous codes a displayed in the PRI TRK GRP NO readout indicator, the ERROR indicator illuminates, and the error message is generated on the local page printer.

93. To terminate the test, press the CONTINUE pushbutton switch and observe that the READY indicator illuminates.

Pushbutton	Status display
READER TO TTY	41
READER TO SP TTY	42
READER TO PUNCH	43
PRINT	44
PUNCH	45
PRINT STOP	46
PUNCH STOP	47
ASSIGN	48
CHANGE	49
DELETE/RESET	50
DISPLAY	51
FACP CLEAR	52
FIELD CLEAR	53
STORE AND REPEAT	54
STORE	55
REMOTE I/O INHIBIT	56
	57
	58
	59
	60
	61
PR ROUTING	62
	63
	64
	65
	66
	67
	68
	69 70
	70
	71
	12
IKN GK METERS	73

94. Press one of the digit pushbuttons listed in the table below and observe that the STATUS digital readout displays the corresponding number listed and all other DRO digits display the selected digit.

Digit pushbutton	Status display
1	74
2	75
3	76
4	77
5	78
6	79
7	80
8	81
9	82
0	83

- 95. Repeat the procedure for each digit listed in any order. To terminate the test, press the CONTINUE pushbutton switch and observe that the READY indicator illuminates.
- 96. Set the FACP INTCP CALLS rotary switch to one of the positions listed in the following chart.

INTCP CALLS switch positions	Status display
OPR	84
INFO	85
ERROR	86

97. Press the ENTER pushbutton switch and observe that the STATUS digital readout indicator display the corresponding number.

98. Press the CONTINUE pushbutton switch and observe that:

- a. PRGM HALT indicator illuminates.
- b. BUS INDICATOR displays a reading of 00011612.
- c. END OF FP message is generated on the local page printer.

	Malfunction	Probable cause	Corrective action
During	FACP lamp test one or more		NOTE
of	the following errors occur.		All replacements are in FACP A7.
a.	Any single indicator fails to light.	a. Defective (1) bulb (2) lamp driver	 a. Replace (1) bulb, retest (2) lamp driver card for falling indicator or group. Repeat test
b.	Any single indicator or group of related indicators fails to light or extinguish.	b. Defective lamp driver.	 Replace lamp driver card for failing indicator indicator or group. Repeat test.
Anv DR	O or related group of DRO's	Defective	Replace
fai	I to display selected digit.	(1) DRO storage(2) DRO address gate.(3) DRO	 (1) DRO storage card. (2) DRO address gate card. Repeat test. (3) DRO. Repeat test.
a.	Any group of DRO's fail to display 000 digit.	a. Defective DRO bus gates.	a. Replace A222 card, repeat test.
b.	AR DRO's fail to display digits 8 and 9.	 b. Defective DRO bus or address gates. (1) DRO bus gates (2) DRO address gates 	 b. Replace gate card: (1) A238 card. Repeat test. (2) A221 card. Repeat test.
C.	All DRO's fail to display a digit 0 through 7.	 c. Defective DRO bus or address gates. (1) DRO bus gates. (2) DRO bus gates. 	 (2) A221 Card. Repeat test. c. Replace gate card: (1) A138 card. Repeat test. (2) A221 card. Repeat test.
d.	Any single DRO or group of DRO's fail to display combina- of numbers not listed above.	<i>d.</i> Defective bus gates.	d. Replace A223 card. Repeat test.
While r	unning FACP off-line test any		
of	following printout occur before ND of FACP TEST printout:		
a.	FP01-XX where XX is 01, 02 or 03.	a. Status register fault.	a. Replace A230 card. Repeat test.
b.	FP01-04.	<i>b. B</i> B failed to set.	b. Replace A230 card. Repeat test.
С.	FP02-XX where XX is 01 or 02.	c. Status register failed to clear,	c. Replace A230 card. Repeat test.
d.	FP03-01.	d. FACP failed to detect program error.	 d. Replace following cards in sequence. Repeat test after each replacement. (1) A238 (2) A233 (3) A227 (4) A127

(5) A140

Malfunction		Probable cause			Corrective action		
e FP04-XX where XX is	s 01 or 02	FAC	P failed to detect program error	e R	Replace A140 card Repeat test		
<i>f.</i> FP04-04.	f.	RRF	F failed to reset.	f. R	Replace A230 card. Repeat test.		
<i>q.</i> FP05-01.	q.	СН	RDY failed to reset.	<i>q.</i> R	Replace A230 card. Repeat test.		
<i>h.</i> FP05-02.	j. h.	Pus	hbutton entry for CONTINUE	<i>h.</i> F	Replace following cards in sequence.		
		faile	d.	R	Repeat test after each card placement.		
				(*	1) Group 1 for CONTINUE switch.		
				ì	2) Group 2 for CONTINUE switch.		
<i>i.</i> FP05-03.	<i>i</i> .	СН	RDY failed to reset.	<i>i.</i> È	Replace A230. Repeat test.		
j. FP06-01. Relate this	printout to j.	Rela	ated to indicator errors recorded	<i>j.</i> R	Replace cards related to errors		
error during test No. 6	6 of	duri	ng test.	re	ecorded during test.		
indicators.		(1)	Lamp gates.	(*	1) Replace following cards in sequence,		
DRO correct but	Indicator				for failing indicator. Repeat test after		
failed.					each replacement.		
					(a) Indicator driver		
					(b) Indicator gate		
					(c) Field Indicator register.		
(2) Incomplete DPO	dicploy with	(2)	Addross counter	1.	(<i>d</i>) CAR decoder.		
(2) Incomplete DRO	lit	(2)	Address counter.	(4	2) Replace following cards in sequence. Repeat test after each replacement		
	п.				(a) $A240$		
					(b) A138		
					(c) A135		
					(d) A136		
					(e) A137		
					(f) A134		
					(<i>g</i>) A140		
					(<i>h</i>) A127		
(3) Incorrect DRO d	isplay with	(3)	Write buffer.	(:	Replace A123 card. Repeat test.		
correct indicator	lit and all						
DRUS III. (4) Incorrect indicate	or lights and	(4)	Indicator addressing	6	4) Replace addressing or switch		
(4) incorrect display a	nnears in	(4)	malcalor addressing.	(-	decoding cards		
wrong DRO's.			(a) Address decoding.		(a) Replace following cards in		
			(<i>ii</i>) · · · · · · · · · · · · · · · · · · ·		sequence. Repeat test after		
					each replacement.		
					1. A237		
					2. A238		
					3. A240		
					4. A243		
			(b) Quitch decedit		5. A239 (b) Banlaga fallowing condition		
			(b) Switch decoding.		(D) Replace following cards in		
					each replacement		
					1 Group 2 for failing switch		
					2. Group 1 for failing switch.		
					3. Group 2 for failing switch.		
					4. Group 3 for failing switch		
(5) No errors record	ed during	(5)	Counter.	(!	5) Replace following cards in		
test.					sequence. Repeat test after		
					each replacement.		
					(a) A240		
					(b) A138		
					(C) A135		
					(a) A136 (a) A137		
					(θ) Α137 (θ) Δ134		
					(a) = A140		
					(h) A127		

k. FP07-01. This printout should only occur when testing ERROR and STORE indicators.

k. ERRF failed to set.

k. Replace A140 card. Repeat test.

	Malfunction		Probable cause		Corrective action
I.	FP07-02. Relate this printout to error recorded during test no.	I.	Related to indicator error recorded during test.	I.	Replace cards related to error recorded during test.
	 (1) DRO correct but indicator failed. 		(1) Lamp gates.		 Replace following cards in sequence, for the failing indicator. Repeat test after each replacement. (a) Indicator driver (b) Indicator gate (c) Field indicator register (d) CAR decoder
	(2) Incomplete DRO display.		(2) Address counter.		 (2) Replace following cards in sequence. Repeat test after each replacement. (a) A240 (b) A138 (c) A135 (d) A136 (e) A137 (f) A134 (g) A140 (b) A127
	(3) Incorrect DRO display with correct indicator lit and all DRO's lit		(3) Write buffer.		(3) Replace A123 card. Repeat test.
	(4) Incorrect indicator lights and		(4) Indicator addressing.		(4) Replace addressing or switch
	wrong DRO's.		(a) Address decoding.		 (a) Replace following cards in sequence. Repeat test after each replacement. 1. A237 2. A238 3. A240 4. A243 5. A239
			(b) Switch decoding.		 (b) Replace following cards in sequence. Repeat test after each card replacement. 1. Group 1 for failing switch. 2. Group 2 for failing switch. 3. Group 3 for falling switch.
	(5) No errors recorded during test.		(5) Address counter.		 (5) Replace following cards in sequence. Request test after each replacement. (a) A240 (b) A138 (c) A135 (d) A136 (e) A137 (f) A134 (g) A140 (b) A127
m.	FP08-01. PRI TRK GR NO displays a 3 digit code.	m.	Incorrect code entry.	m.	 (11) 5127 Repeat test to insure you made correct entry, then replace following cards in sequence. Repeat test after card replacement. (1) Group 1 for failing switch. (2) Group 2 for failing switch. (3) Group 3 for failing switch
n.	FP08-02. Relate this printout to errors recorded during test no. 8 of indicators	n.	Related to indicator errors recorded during test.	n.	Replace cards related to error recorded during test.
	(1) DRO correct but indicator failed.		(1) Lamp gates.		 Replace following cards in sequence, for the failing indicator. Repeat test after each replacement.

Malfunction	Probable cause	Corrective action
(2) Incomplete DRO display.	(2) Address counter.	 (a) Indicator driver (b) Indicator gate (c) Field indicator register (d) CAR decoder (2) Replace following cards in sequence. Repeat test after each replacement. (a) A240 (b) A138 (c) A135 (d) A136 (e) A137 (f) A134 (g) A140 (b) A127
(3) Incorrect DRO display with correct indicator lit and all	(3) Write buffer.	(3) Replace A123 card. Repeat test.
DRO's lit. (4) Incorrect indicator lights and correct display appears in wrong DRO's.	(4) Indicator addressing.(a) Address decoding.	 (4) Replace addressing or switch decoding. (a) Replace following cards in sequence. Repeat test after each replacement. 1. A237 2. A238 3. A240 4. A243 5. A230
	(b) Switch decoding.	 b) Replace following cards in sequence. Repeat test after each card replacement 1. Group 1 for failing switch. 2. Group 2 for failing switch. 3. Group 3 for failing switch.
(5) No errors recorded during test.	(5) Address counter.	 (5) Replace following cards in sequence Repeat test after each replacement. (a) A240 (b) A138 (c) A135 (d) A136 (e) A137 (f) A134 (g) A140 (h) A127
o. FP08-03 p. FP08-77 q. FP09-01	 o. BB failed to set p. CH RDY failed to set. q. Incorrect digit entry. 	 Replace A230 card. Repeat test. Replace A230 card. Repeat test. Replace following cards in sequence. Repeat test after each card replacement. (1) Group 1 for failing digit (2) Group 2 for failing digit (3) Group 3 for failing digit
r. FP09-02	r. Address counter.	 <i>r.</i> Replace following cards in sequence. Repeat test after each replacement. (1) A240 (2) A138 (3) A135 (4) A136 (5) A137 (6) A134 (7) A140

(7) A140(8) A127

	Malfunction		Probable cause		Corrective action
S.	FP09-03. Relate this printout to errors recorded during test no.	S.	Related to indicator errors recorded during tests.	S.	Replace cards related to error recorded during test.
	9 of indicators. (1) Odd digits fail.		(1) Switch decoding.		 Replace following cards in sequence. Repeat test after each replacement. (a) A114 (b) A109
	(2) Digits 4, 5, 6, and 7 failing.		(2) Switch decoding.		 (2) Replace following cards in sequence. Repeat test after each replacement. (a) A103 (b) A104
	(3) Random digit errors.		(3) Switch decoding.		 (3) Replace following cards in sequence. Repeat test after each replacement. (a) A103 (b) A104 (c) A114 (d) A109
	(4) No errors recorded during test.		(4) Address counter.		 (4) Repeat following cards in sequence. Repeat test after each replacement. (a) A240 (b) A138 (c) A135 (d) A136 (e) A187 (f) A134 (g) A140 (h) A127
t. u.	FP09-04 FP10-01. PRI TRK GR NO displays 3 digit code. Relate printout to errors recorded during test no. 10 of indicators.	t. u.	CH RDY failed to set. Incorrect command entry.	t. u.	Replace A230 card. Repeat test. Repeat test to insure you make the correct entry.
	(1) INTCP CALLS OPR fails.		(1) Switch decoding.		 Replace following cards in sequence. Repeat test after each card replacement. (a) Group 1 for OPR switch. (b) Group 2 for OPR switch (c) Group 3 for OPR switch.
	(2) INTCP CALLS INFO fails.		(2) Switch decoding.		 (2) Replace following cards in sequence. Repeat test after each card replacement. (a) Group 1 for INFO switch. (b) Group 2 for INFO switch
	(3) INTCP CALLS ERROR fails.		(3) Switch decoding.		 (3) Replace following cards in sequence. Repeat test after each card replacement. (a) Group 1 for ERROR switch. (b) Group 2 for ERROR switch. (c) Group 3 for ERROR switch.
v.	FP10-02	u.	Address counter.	V.	 Replace following cards in sequence. Repeat test after each replacement. (1) A240 (2) A138 (3) A135 (4) A136 (5) A137 (6) A134 (7) A140 (8) A127
<i>W</i> .	FP10-77	W.	CH RDY failed to set.	W.	Replace A230 card. Repeat test.

		DRO	DRO	Address
DRO		address	store	gate
TERMINAL NO	UNITS	4A0	A211	A202
	TENS	4A1	A211	A202
	HUNDREDS	4A2	A211	A202
	THOUSANDS	4A3	A211	A202
TERMINAL TYPE	UNITS	2A0	A207	A216
	TENS	2A1	A207	A216
CLASSCODE	UNITS	2B0	A207	A216
	TENS	2B1	A207	A216
DIR NO/TRK GP NO	UNITS	3A0	A208	A218
	TENS	3A1	A209	A218
	HUNDREDS	3A2	A209	A219
CONF/GR MIN CT	UNITS	2C0	A207	A217
	TENS	2C1	A208	A217
MODE II TERM NO	UNITS	4B0	A212	A203
	TENS	4B1	A212	A203
	HUNDREDS	4B2	A212	A203
	THOUSANDS	4B3	A212	A203
SPCI_CKT_NO/PR_NP/SI_NO	UNITS	200	A208	A217
	TENS	2D1	A208	A217
STATUS/LINE GR NO/ALTN	UNITS	2E0	A208	A218
SI NO	TENS	2E1	A208	A218
FUNCTION CODE/RANK		140	A207	A202
PRI TRK PP NO	UNITS	380	A209	A219
	TENS	3B1	A209	A219
	HUNDREDS	382	A209	A219
ALTN TRK GP NO	UNITS	300	A209	A204
	TENS	301	A211	A204
	HUNDREDS	302	Δ211	Δ203
FIXED DIR NO/TREC ONT	UNITS	540	A212	A200
	TENS	541	Δ212	Δ204
	HUNDREDS	542	Δ212	Δ204
	THOUSANDS	543	Δ213	A204
		544	A213	A204 A206
		74	A213 A214	A200
FR-3L-777/1017-7777		7.44	AZ14 A214	A200
		745	A214 A214	A200
		740	A214	A200
		7 AU	HZIJ 1010	A200 A205
		741	HZ IS	A200
		7A2	A213	A205
	THOUSANDS	7A3	A214	A205

Section IV. DRO CARD REPLACEMENT

Section V. INDICATOR CARD REPLACEMENT

				Field	
	Indicator	Lamp	Lamp	indicator	CAR
Indicator	address	driver	gate	register	decoder
TERMINAL NO	ID 204	A153	A149		
TERMINAL TYPE	ID 202	A152	A150		
CLASSCODE	ID 212	A152	A150		
DIR NO	ID 203	A153	A149		
TRK OR NO	ID 213	A153	A149		
CONF	ID 222	A152	A150		
GR MIN COUNT	ID 242	A152	A160		
MOD II TERM NO	ID 214	A153	A148		
SPCL CKT NO	ID 252	A152	A150		
PR NO	ID 262	A152	A150		
SL NO	ID 272	A152	A150		
STATUS	ID 302	A153	A150		
LINE OR NO	ID 232	A152	A150		
ALTN SL NO	ID 312	A153	A151		
FUNCTION CODE	ID 201	A152	A151		

					Field	
		Indicator	Lamp	Lamp	indicator	CAR
Indicator		address	driver	gate	register	decoder
RANK		ID 211	A152	A151		
PRI TRK GR NO		ID 223	A153	A149		
ALT TRK GR NO		ID 233	A153	A149		
FIXED DIR NO/TRFC CNT		ID 205	A153	A148		
PR-SL-XXX/NNX-XXXX		ID 207	A153	A148		
NARROWBAND	TOTAL	ID 206	A153	A147		A237
	FO	ID 216	A153	A147		A237
	FLASH	ID 226	A153	A147		A237
	IMMED	ID 236	A153	A147		A237
	PRI	ID 246	A153	A147		A237
WIDEBAND	TOTAL	ID 256	A153	A147		A237
	PREC	ID 266	A153	A147		A237
OPERATORS	CALLS	ID 276	A154	A147		A237
	RECALLS	ID 306	A154	A147		A231
	INFO	ID 326	A154	A147		A237
	INTCP	ID 316	A154	A147		A237
TRUNK GR TRAFFIC	INCOM	ID 336	A154	A146		A237
	OUTGO	ID 346	A154	A146		A237
	PRMPT	ID 356	A154	A146		A237
	ATB	ID 366	A154	A146		A237
	LKOUT	ID 376	A154	A146		A237
READY		ID 220	A152	A148		
ERROR		ID 230	A152	A148		
STORE		ID 240	A152	A148		
READER TO TTY			A152		A144	
READER TO SPTTY			A152		A144	
READER TO	PUNCH		A152		A144	
INTCP CALLS	ENTER		A152		A146	

Section VI. PUSHBUTTON CARD REPLACEMENT

Pushbutton	Code	Group 1	Group 2	Group 3
READER TO TTY	041	A113, A103,	A109, A113	
READER TO SPTTY	042	A114, A108 A113, A103,	A107, A104,	
READER TO PUNCH	043	A114, A108 A113, A103,	A109 A107, A104,	A133
PRINT	044	A114, A108, A113, A103,	A109 A107, A104	A109, A133
	045	A114, A108 A113 A103	A107 A104	
	040	A114, A108		
PRINT STOP	046	A113, A103, A114, A108	A107, A104	
PUNCH STOP	047	A113, A103, A114, A108	A107, A104	A109, A133
ASSIGN	101	A132, A133, A114	A109	
CHANGE	102	A132, A133, A114	A107, A103, A104, A108	
DELETE/RESET	103	A132, A133, A114	A107, A103, A104 A108	A109 A104 A108
DISPLAY	104	A132, A133, A114	A107, A103, A104,	
FACP CLEAR	105	A132, A133, A114	A107, A110, A104	A109
FIELD CLEAR	106	A132 A133 A114	A108 A107 A103	
STORE AND REPEAT	107	A132, A133, A114	A107, A103, A104, A108	A109

Pushbutton	Code	Group 1	Group 2	Group 3
STORE	110	A132, A133,	A113, A109,	
	111	A114 A132 A133	A108	
CONTINUE		A132, A133, A114	A103, A109, A108	
TERMINAL SERVICE	141	A132, A133,	A113, A103,	A109
TERMINAL NO ASGMT	142	A114 A132 A133	A108 A113 A103	A107 A104
		A114	A108	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
DIRECTOR NO ASGMT	143	A132, A133,	A113, A103,	A107, A104,
TRK GR NO	144	A114 A132, A133,	A108 A113, A103,	A109 A107, A104
		A114	A108	
PR ROUTING	145	A132, A133, A114	A113, A103, A108	A107, A104, A109
SL ROUTING	146	A132, A13,	A113, A103,	A107, A104
	4 47	A114	A108	A407 A404
ALTN SE ROUTING	147	A132, A13, A114	A113, A103, A108	A107, A104, A109
OP/JXX ROUTING	150	A132, A133,	A113, A103,	
	151	A114 A132- A133	A108, A109	
	101	A114	A108, A109	
PRST CONF ENTRY	152	A132, A133,	A113, A103,	A107, A104
LINE GR ENTRY	153	A114 A132 A133	A108, A109 A113 A103	Δ107 Δ104
	100	A114	A108, A109	///07, ///04
DAC ROUTING	154	A132, A133, A133,	A113, A103,	A107, A104
TRUNK TEST	155	A114 A132, A133,	A108, A109 A113, A103,	A107, A104
		A114	A108, A109	,
STATUS156	A132, A133,	A113, A103	A113, A103 A108 A109	A104
TRAFFIC METERS	157	A132, A133,	A113, A103,	A107, A104
	400	A114	A108, A109	
IRK GR METERS	160	A132, A133, A114	A113, A103, A108	
REMOTE I/O INHIBIT	201	A132, A103,	A109, A133,	
	202	A108 A132 A103	A114 A107 A104	
	202	A108	A107, A104	
INTCP CALLS OPR	203	A132, A103,	A107, A104	A109, A133,
INTCP CALLS INFO	204	A108 A132, A103,	A107. A104	A114
		A108		
INTCP CALLS ERROR	206	A132, A103,	A107, A104	A109, A133,
ENTER	210	A100		A114
0	240	A400 A400 A400		
2	241 242	A132, A103, A108 A132 A103 A108	A109, A133, A114 A107 A104	
3	243	A132, A103, A108	A107, A104	A109, A133, A114
4	244 245	A132, A103, A108	A107, A104	A100 A133 A114
6	240	A132, A103, A108	A107, A104	A103, A133, A114
7	247	A132, A103, A108	A107, A104	A109, A133, A114
8 9	260 251	A132, A103, A108 A132, A103, A108	A113, A109 A113, A109	A133, A114
			,	

EXHIBIT G

BOOTSTRAP DIAGNOSTIC PROGRAM

Section I. GENERAL

The Bootstrap diagnostic program exercises the fundamental logic in the Central Processor and its associated memory. The program is divided into three sections: the first section checks the basic ability of the processor to read the loader and bootstrap program into memory, assuming that the preloader was successfully loaded. The second section checks out a few basic instructions and the fundamental capacity of the registers. The third section programs more comprehensive checks, interrupt checks and memory checks. Program halts are the key identifying output of each section. It must be noted that the Bootstrap diagnostic program destroys the contents or memory so that preloader and loader

instructions must be reentered to continue testing.

Section II. DIAGNOSTIC PROGRAM

THE FOLLOWING PROCEDURES ARE USED TO CONVERT THE OPERATIONAL PRELOADER PROGRAM TO THE OFF-LINE DIAGNOSTIC PRELOADER PRELOADER PROGRAM

- 1. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 2. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 3. Set the WSR toggle switches to 0027760.
- 4. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 5. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A.
- 6. Set the WSR toggle switches to 55137754.
- 7. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified on the on-line program preloader instruction entries chart below. If the entries do not agree, or are absent, the on-line program preloader instructions must be loaded into memory before proceeding. If the entries appearing in parenthesis on the chart are already loaded into memory, proceed to step 42 below.
- 8. Set the MEMORY guarded switch to the UNPROTECTED position.
- 9. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.

Address	Instruction
00277750	01077751
00277751	00002404
00277752	05200377
00277753	24077755
00277754	22077750
00277755	70100000
00277756	7000001
00277757	01077760
00277760	00002400
00277761	02200040
00277762	24077757
00277763	0 377764
00277764	00002404
00277765	34000020
00277766	35000010
00277767	7200001
00277770	7400003
00277771	22077757
00277772	62501776 (62500476)
00277773	72100001
00277774	74100107 (4100235)
00277775	22077756
00277776	0000000

- 10. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 11. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 12. Verify that the CLOCK OPERATE CONTROL rotary switch is in the CONT position.
- 13. Press the CLEAR pushbutton switch.
- 14. Set the WSR toggle switches to 00277750.
- 15. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 16. Set the OPERATIONAL CONTROL rotary switch to STORE SEQL and the REGISTER SELECT to MEM.
- 17. Set the WSR toggle switches to the instruction entries listed in the on-line preloader instruction chart and press the INITIATE pushbutton switch after each setting. Observe that the BUS INDICATOR displays the entered instruction.
- 18. Press NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator lights.
- 19. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 20. Set the WSR toggle switches to 00277750.
- 21. Press the INITIATE pushbutton switch and observe that BUS INDICATOR displays the address listed.
- 22. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A. 23. Set the WSR toggle switches to 55137754.
- 24. Press INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified on the chart.

NOTE

The following procedures will correct an erroneous address entered from the chart of specified addresses and instructions.

- a. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- b. Set the ASR toggle switches to the correct address.

- c. Press INITIATE pushbutton switch and observe that the BUS INDICATOR displays the correct address.
- *d.* Set the WSR toggle switches to the *correct instruction number*.
- e. Set the OPERATIONAL CONTROL rotary switch to STORE.
- f. Press INITIATE pushbutton switch and observe BUS INDICATOR displays the correct instruction.
- g. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- *h.* Press INITIATE pushbutton switch and verify that the BUS INDICATOR displays the correct instruction.
- 25. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 26. Set the MEMORY guarded switch to the UNPROTECTED position.
- 27. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- 28. Set the ASR toggle switches to 277772.
- 29. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62501776.
- 30. Set the WSR toggle switches to 6400476.
- 31. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 32. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62500476.
- 33. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62500476.
- 35. Set the ASR toggle switches to 277774.
- 36. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100107.
- 37. Set the WSR toggle switches to 74100235.
- 38. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 38. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100235.
- 40. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 41. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100235.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE OFF LINE DIAGNOSTIC LOADER PROGRAM INTO MEMORY

- 42. Load the off-line diagnostic loader tape (SM-D-752126) on the paper taps reader.
- 43. Set the paper tape reader MODE SELECT toggle switch to STRIP and the PWR switch to ON.
- 44. Set the system status panel RESET SELECT TAPE READER toggle switch to ON.
- 45. Press the system status panel RESET pushbutton switch several times and observe that the loader moves.
- 46. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT Indicator illuminates.
- 47. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 48. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 49. Set the WSR toggle switches to 00277750.
- 50. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 51. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 52. Set the RUN/ONE INSTR toggle switch to RUN.
- 53. Press the INITIATE pushbutton switch and observe that:
 - a. Off-line diagnostic loader tap strip loads into memory.
 - b. PRGM HALT indicator illuminates at the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00277777.

- 54. Rewind the loader tape by setting the system status panel TAPE READER REWIND toggle switch to ON.
- 55. Set the PARITY ERROR HALT toggle switch to ON.
- 56. Set the CLOCK OPERATE CONTROL rotary switch to CONT.
- 57. Set the ADV-RPT toggle switch to ADV.
- 58. Set the REAL TIME CLOCK guarded switch to the DISABLE position.
- 59. Set the REGISTER SELECT rotary switch to PEX.
- 60. Set the CONTROL TRANSFER toggle switch to DISABLE.
- 61. Set the printer motor control BYPASS toggle switch to BYPASS.
- 61.1. Set the MEMORY guarded switch to the UNPROTECTED position.

THE FOLLOWING PROCEDURES LOAD THE DIAGNOSTIC PROGRAM INTO MEMORY

- 62. Load the Bootstrap (SM-D-751714) and Maintenance Control Panel (SM-D-741718) Diagnostic Program tapes on the paper tape reader.
- 63. Set the paper tape reader MODE SELECT toggle switch to REEL and the PWR switch to ON.
- 64. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates and the PRGM HALT indicator extinguishes.
- 65. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 65. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 66. Set the WSR toggle switches to 00000500.
- 67. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00000500.
- 68. Press the system status panel RESET pushbutton switch several times and observe that the diagnostic tape moves.
- 69. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 70. Press the INITIATE pushbutton switch and observe that:
 - a. Segment A of the diagnostic program tape loads into memory.
 - b. PRGM HALT indicator illuminates at the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00000631.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE STARTING ADDRESS INTO THE PROGRAM COUNTER

- 71. Set the REGISTER SELECT rotary switch to PEX.
- 72. Press the NORMAL HALT pushbutton switch and observe the PRCS HALT indicator illuminates.
- 73. Press the CLEAR pushbutton switch.
- 74. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 75. Set the WSR toggle switches to 00001051.
- 76. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00001051.
- 77. Set the WSR toggle switches to all zeros.
- 78. Set the ASR toggle switches to all zeros.

THE FOLLOWING PROCEDURES ARE USED TO EXECUTE THE SECOND SECTION OF THE BOOTSTRAP ROUTINES

- 79. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 80. Press the INITIATE pushbutton and observe that the PRGM HALT indicator illuminates and the BUS INDICATOR displays a reading of 00001053. (This showed that the program successfully executed a TRU and HLT instruction.)
- 81. Press the INITIATE pushbutton and observe that the PRGM HALT indicator Illuminates and the BUS INDICATOR displays a reading of 00002540.

THE FOLLOWING PROCEDURES ARE USED TO EXECUTE THE THIRD SECTION OF THE BOOTSTRAP ROUTINES

- 82. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates and the PRGM HALT indicator extinguishes.
- 83. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 84. Set the WSR toggle switches to 0000506.
- 85. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00000506.
- 86. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 87. Press the INITIATE pushbutton switch and observe:
 - a. Segment B of the diagnostic program tap loads into memory.
 - b. PRGM HALT indicator illuminates at the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00000631.
- 88. Set the REGISTER SELECT to PEX.
- 89. Press the NORMAL HALT pushbutton switch and observe the PRCS HALT indicator illuminates.
- 90. Press the CLEAR pushbutton switch.
- 91. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 92. Set the WSR toggle switches to 00003562.
- 93. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 000562.
- 94. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 95. Set the WSR toggle switches to all zeros.
- 96. Press the INITIATE pushbutton and observe that the PRGM HALT Indicator illuminates and the BUS INDICATOR displays a reading of 0000513.
- 97. Set the PARITY ERROR HALT toggle switch to OFF and the REAL TIME CLOCK guarded switch to ENABLE.
- 98. Press the INITIATE pushbutton and observe that the PRGM HALT indicator illuminates and the BUS INDICATOR displays a reading of 00206547.

Section III. BOOTSTRAP LOADING HALT TABLE

a. Section I.

Halt Location	Test Description	Test Result	Further Checks
00000- 001050 001053- 001055 377777 001052	Following halt may occur while loading the bootstrap diagnostic program. Program halt.	Address bit(s) lost. AC to PC transfer failed. Address bit(s) picked up.	Press INITIATE to start test section B.
<u>b</u> . Section II.			
Halt Location	Test Description	Test Result	Further Checks
001271 001223	 (1) Car Accumulator Check. (a) Check sign bit. (b) Check is 01-23. 	A00 cannot be cleared. Bit in A cannot be cleared.	Display A to determine failing bit.
001277	 (2) CLA Instruction Check, Memory Access. (a) CLA a word coins all zeros. (b) CLA a word containing 37777777. If transfer fails, CLA a constant of 77777. If both CLA 	Zeros transfer from memory failed.	Display A and B to determine failing bits.
001305 001310 001311	(c) CLA a word with only one bit set. Repeat for all	CLA failed. CLA a constant succeeded. CLA and CLA a constant failed. LGE succeeded. All instructions failed.	
001372	bit positions (00-23).	A00 not transferred.	Display A and B to determine where bit was
001373- 001421	(3) CLA Instruction Check, No Memory Access	Bit not transferred. Symbolic address indicates bit that failed (01-23).	Display A and B to determine where bit was lost.
001425	(a) CLA a constant of 77777.	No hits transferred.	

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Halt Location	Test Description	Test Result	Further Checks
	(b) CLA a constant with only one hit set. Repeat		
001465-001503	for fifteen bit positions (09-23).	Bit not transferred. Symbolic address indicates bit that failed (09-23).	
	 (4) LGE Instruction Check. (a) LGE a word containing all zeros with A = 0. 		
001507		Bit other than 00 failed.	Display A and B to determine bit that failed.
001512	(<i>b</i>) LGE a word containing all zeros with A =	Only bit 00 failed.	
001517	//////.	Bits 101-23 failed.	
	(<i>c</i>) LGE a word containing all ones with A = 7777777.		
001524		Bits 01-23 failed.	
	(<i>d</i>) LGE a word with only one bit set with $A = 0$. Repeat for all bit positions (00-23).		
001635		Bit 00 failed.	
01664		failed (01-23).	
	(e) Set only one bit A, LGE with a word containing all zeros. Repeat for each bit position (A00-A23).		
001775		Bit 00 failed.	
001776- 02024		Bit failed. Symbolic address indicates bit that failed (01-23).	
	(<i>f</i>) LGE a word containing all ones with A = 7777777.		
002030		Bit failed.	Display A and B to determine bit that failed.
002033	(5) I GM Instruction Check	Bit 00 failed.	
	(a) LGM a word containing all ones with $A = 0$.		
002040	(<i>b</i>) LGM a word containing all zeros with A =	Bit failed.	Display A and B to determine bit that failed.
002045	///////.	Bit failed	Display A and B to determine bit that failed
002070	(<i>c</i>) LGM a word containing all ones with A = 777777777, then LGE results with a word containing all ones.		Display A and D to determine bit that failed.

Halt Location	Test Description	Test Result	Further Checks
002033		Bit failed.	Display A to identify bit that failed.
	(6) LGA Instruction Check. (a) LGA a word containing 40000000 with A = 0.		
002056		Bit 00 failed.	
	(b) LGA a word containing 40000000 with A = 40000000 .		
002061		Bit 00 failed.	
	(c) LGA a word containing all zeros wit A = 77777777, then LGE the results with a word containing all ones		
002066		Bit failed.	Display A to determine bit that failed.
	(d) LGA a word containing all ones with $A = 0$, then LGE the results with a word containing all ones.		
002073		Bit failed.	Display A to determine bit that failed.
	(e) LGA a word containing 25252525 with A = 5252525252, then LGE results with a word containing		
002100	all ones.	Bit failed.	Display A to determine bit that failed.
	(<i>f</i>) LGA a word containing 52525252 with A = 25252525, then LGE results with a word containing		
002105	all ones.	Bit failed.	Display A to determine bit that failed.
	(g) LGA a word containing 2525252 with $A = 0$, then LGE results with a word containing 52525252.		
002112		Bit failed.	Display A to determine bit that failed.
	(<i>h</i>) LGA a word containing 25252525 with $A = 0$, then LGE results with a word containing 25252525.		
002117		Bit ailed.	Display A to determine bit that failed.
	 (7) TRP Instruction Check. (a) CLA a word containing all ones then execute TRP 		
002123		TRP succeeded with $A00 = 1$.	Display A for $A00 = 1$.

Halt Location	Test Description	Test Result	Further Checks
	(<i>b</i>) CLA a word containing all zeros, then execute TRP.		
002126	(0) Posister Charle	TRP failed with $A00 = 0$.	Display A for $A00 = 0$.
	CLA each CPU register and check contents.		Display A to determine bits that failed.
	č	BR ≠ 0.	
		Q ≠ 0.	
		RTC≠0. SBR≠0	
		$AR \neq 0.$	
		LSR ≠ 0.	
		CPD incorrect.	
	(9) STR Instruction Check, Part 1.		
	(a) STR a word containing all ones to location		
	001141. If transfer fails STR a word containing all ones to O If second STR fails RPA a word		
	containing all ones to Q.		
002226		STR To 001141 failed.	
002233		STR to Q succeeded. Both STR attempts failed	
002200		RPA succeeded.	
002234	(b) If CTD to 1111 averaged at test high and a bit	All instructions failed.	
	(0) ITSTR to TT4T succeeded, test high order bits (00-08). LGM the contents of location 1141 with a		
	word containing 77700000.		
002237		Bit 00 failed.	Display A to determine bit (01.09) that failed
002242	(c) If high order bit test succeeds test low order bits	Bit (11011101-001 Talled.	Display A to determine bit (01-00) that failed.
	(09-23). LGM the contents of location 001141 with		
	a word containing 00077777. If transfer failed RPA		
002253		STR to 001141 failed.	Display A to determine bit (09-23) that failed.
000054		RPA succeeded.	
002254		STR and RPA failed to load low order bits (09- 23) in location 001141	
	(10) RPA/STA Instruction Check.		
	(a) RPA a word containing 00077777 to location		
002263	001141.	RPA failed.	

Halt Location	Test Description	Test Result	Further Checks
	(b) RPA a word containing all ones to location		
002272 002275	001141.	Bit 00 was changed during RPA. Bits 01-08 were changed during RPA.	
002304	(<i>c</i>) STA a word containing all ones to location 001141.	Rite 00-08 failed to clear on STA instruction	Display A to determine hits that failed
002304	 (11) STR Instruction Check Part 2. (a) STR a word containing all ones in location 001141. If transfer fails STR to Q. If STR to location 001141 fails and STR to Q succeeds load contents of location 001141 in A. 		
002322 002324		Both instructions failed. STR to location 001141 Failed. STR to Q	Display A to determine bit(s) that failed.
	(b) STR a word containing all zeros in location	succeeded.	
002333	001141.	STR failed.	Display A to determine bits that failed.
	 (12) Memory Check, Addresses 003561 to 006500. (a) Each memory location tested has its address written into it. Each location is then read to verify the contents. 		
002406		Defective location was found.	Display A for address of defective location. Note A00 = 1.
	(b) When testing is resumed, the program will halt when the next highest good location is found.		
002424		First good location after BB470 halt.	Display A for address of first good location found since last BB470 halt.
	 (c) When testing is resumed, the program will halt when the next highest defective location found (BB470 halt). Alternate halts for defective and nondefective locations continues until location 006500 is checked. (d) Each memory location has the compliment of its address written into it. Each location is then read to verify the contents. 	Note AUU = 0.	

Halt Location	Test Description	Test Result	Further Checks
002302		Defective location was found.	Display A for address of first good location. Note $A00 = 1$.
002521	(<i>e</i>) When testing is resumed, the program will halt when the next highest good location is found.(<i>f</i>) When testing is resumed, the program will halt when the next highest defective location is found.	First good location found after (BB490) halt.	Display A for address of first good location found after last BB490 halt. Note A00 = 0.
	(BB490 halt). Alternate halts for defective location is found. defective location continue until location 006500 is checked.		
002536		Errors were found during memory test. These tests must run error free before further tests can be made.	
002537		Memory test successfully completed. Load remainder of bootstrap test.	
<u>c</u> . Section III			
Halt	T (D) (<i>d</i>)	T (D)	
Location	Test Description	Test Result	Further Checks
	 (1) Register Gating Checks. (a) STR a word containing all ones to A. A check is made to insure Q gating was not enabled. 		
004134	(<i>b</i>) STR a word containing all ones to Q. Check is made of remaining registers to determine if any other gates were enabled.	STR to A also enabled Q gates.	
004142		BR gates enabled.	Display BR.
004145		EIC gates enabled.	Display RTC.
004152		IAR dates enabled	Display SBR. Display IAR
004164		OAR gates enabled.	Display OAR.
004170		LSR gates enabled.	Display LSR.
004175		CPS gates enabled.	Display CPS.
004202		CPD gates enabled.	Display CPD.
	(c) STR a word containing all ones to OAR. A check is made of remaining registers to determine if any other gates were enabled.		
004211	,	BR gates enabled.	Display BR.

Halt Location	Test Description	Test Result	Further Checks
004215 004221 004226 004232 004236 004243 004250	(<i>d</i>) CLA a word containing all on from A. If transfer	RTC gates enabled. SBR gates enabled. JAR gates enabled. Q gates enabled. LSR gates enabled. CPS gates enabled. CPD gates enabled.	Display RTC. Display SBR. Display JAR. Display Q. Display LSR. Display CPS. Display CPD.
	succeeds CLA a word containing 77777777 from		
004262 004272	۵.	CLA from A and OAR both failed. CLA from A failed. CLA from OAR succeeded. CLA from Q failed	
004273		CLA from A failed. CLA from OAR and Q both succeeded.	
	(e) CLA WORD SWITCH REGISTER check for all ones or all zeros.		
004277		WORD SWITCH REGISTER not all ones.	Set WORD SWITCH REGISTER to all ones or all zeros.
004304	(<i>f</i>) STR a word contains 37777777 to CPD. Check if transfer fails CLA a word containing all on from OAR. If STR to CPD succeeds, check status of bit 00 on CLA from CPD.	WORD SWITCH REGISTER not all zeros.	Press NORMAL HALT then INITIATE.
004314		STR to CPD failed. CLA from OAR succeeded.	
004322		Bit 00 picked up on STR to CPD.	
004331	 (g) STR a word containing 40000000 to CPD. (h) STR a word containing all ones to Q. If transfer fails, LDQ with a memory location containing all ones. 	Bit 00 lost or bit picked up on STR to CPD.	
004342 004343		STR to Q failed. LDQ succeeded.	
004347	(i) STR a word containing all zeros to Q.	Bit failed in STR to Q.	Display A to determine bit that failed.

Halt Location	Test Description	Test Result	Further Checks
004354	(A GTD a word containing 27777777777 to CDC	Bit in Q cannot be cleared.	Display A to determine bit that failed.
004364	()) STR a word containing 37777777 to CPS.	Bit lost in STR to CPS.	Display A to determine bit that failed. (Lost bit $= 1.$)
004372	STR a word containing all zeros to CPS. (<i>k</i>) STR a word containing 77777660 to RTC. If transfer fails CLA from PC	Bit failed to clear in CPS.	Display A to determine bit that failed.
004403 004404 004407	 (2) Interrupt Checks. (a) STR a word containing 20000000 to CPS. STR 	STR to RTC failed. CLA from PC succeeded. Both instructions failed. Bit failed on STR to RTC.	Display A to determine contents of RTC. Display A to determine bit that failed.
004425 004431	a word containing 60000000 to CPD. Check for interrupt.	Bus 01 failed to interrupt. Incorrect PC stored on interrupt.	Display location 0001042 to determine PC contents stored in interrupt.
004445	 a word containing 50000000 to CPD. Check for interrupt. (<i>c</i>) STR a word containing 04000000 to CPS. STR a word containing 44000000 to CPD. Check for interrupt. 	Bus 02 failed to interrupt.	
004460	(<i>d</i>) STR a word containing 02000000 to CPS. STR a word containing 42000000 to CPD. Check for interrupt	Bus 03 failed to interrupt.	
004473	(e) STR a word containing 01000000 to CPS. STR a word containing 41000000 to CPD. Check for interrupt.	Bus 04 failed to interrupt.	
004506	·········	Bus 05 failed to interrupt	

Halt			
Location	Test Description	Test Result	Further Checks
	(<i>f</i>) STR a word containing 00400000 to CPS. STR a word containing 40400000 to CPD. Check for interrupt		
004521	(g) STR a word containing 0020000 to CPS. STR a word containing 40200000 to CPD. Check for interrupt.	Bus 06 failed to interrupt.	
004534		Bus 07 failed to interrupt.	
	(<i>h</i>) STR a word containing 00100000 to CPS. STR a word containing 40100000 to CPD. Check for interrupt.		
004547	·	Bus 08 failed to interrupt.	
	 (i) STR a word containing 00040000 to CPS. STR a word containing 40040000 to CPD. Check for interrupt. 		
004562		Bus 09 failed so interrupt.	
	(<i>j</i>) STR a word containing 00020000 to CPS. STR a word containing 40020000 to CPD. Check for interrupt.		
004575		Bus 10 failed to Interrupt.	
	(<i>k</i>) STR a word containing 00010000 to CPS. STR a word containing 40010000 to CPD. Check for interrupt.		
004610		Bus 11 failed to interrupt.	
	 (1) STR a word containing 00000200 to CPS. STR a word containing 40000200 to CPD. Check for interrupt. 		
004623		Bus 16 failed to interrupt.	
004627	(<i>m</i>) Attempt to execute an illegal instruction - 11004637. Check for interrupt.	CPD 00 failed to reset alter Interrupt occurred.	
004637	·	Interrupt failed.	
004651		Incorrect CPS bit set for illegal instruction interrupt.	Display A to determine bit set.
	(3) <i>Interrupt Errors.</i> One of following halts occurs during normal testing.		

Halt Location	Test Description	Test Result	Further Checks
004673		Instruction parity error occurred.	IPE is printed. Display A for address of instruction causing error
004712 004737		Date parity error occurred. Illegal instruction was decoded.	DPE is printed. ILI is printed. Display A for address of instruction causing error.
004756 004772		Remote teletype interrupt occurred. Memory protect violation occurred.	IO is printed. CXR is printed. Display A for address violated.
005015 005030 005032 005045		Control transfer initiated. Spare teletype interrupt occurred. Interrupt occurred from unknown source. Program should resume after halt. Failure indicates halt interrupt did not occur	CXR is printed. RTC is printed. Display A for PC contents at time of interrupt.
005056 005063 005101		Unintentioned halt interrupt occurred. CPD 09 not set. Program halt failed. Timeout interrupt failed when nonexistent device is addressed.	Display A for PC contents at time of interrupt. IO CHECK is printed.
005173	(4) Real Time Clock Checks.	RTC Is running with REAL TIME CLOCK switch	
005122	Program halt. Set PARITY ERROR HALT switch to OFF, set REAL TIME CLOCK switch to ENABLE		
005202 005205 005221 005231 005255		RTC overflow occurs too quietly. RTC was not reset on overflow. RTC operating excessively fast. RTC operating fast. RTC overflow interrupt failed or RTC running slightly slow.	
	 (5) Memory Check Locations 00000-003561 and 006500-37737. (a) Each memory location tested has its address written into it. Each location is then read to verify the contents 		
005322		Interrupt location (001043) written into.	Location 001043 should contain 22004660 (INIT).
		Display A to determine actual contents of location 001043.	
005351		Defective memory location found.	Display A for address of defective location. Note A00 =1. To loop on defective location press NORMAL HALT then INITIATE.

Halt Location	Test Description	Test Result	Further Checks
005371	(<i>b</i>) When testing is resumed the program will halt when the next highest god location is found.	First good location after BC680 halt.	Display A for address of first good location found since last BC680 halt. Note A00 = 0.
	 (c) When testing is resumed, the program will halt at the next highest defective location (BC680 halt). Alternate halts for defective and non-defective locations continue until location 37737 is checked. (d) Each memory location has the complement of its address written into it. Each location is then read to verify the contents. 		
005521		Interrupt location (001043) written into.	Location 001043 should contain 22004660 (INT). Display A to determine actual contents of 001043.
005554	(e) When testing is resumed the program will halt when the next highest good location is found.	Defective memory location found.	Display A for address of defective location. Note A00 = 1. To loop on defective location press NORMAL HALT, then INITIATE.
005575		First good location after BC710 halt.	Display A for address of first good location found since last BC680 halt. Note A00 = 0.
	 (f) When testing is resumed, the program will halt at the next highest defective location (BC710 halt). Alternate halts for defective and non-defective locations continues until location 37737 is checked. (6) Index Register Checks. (a) Set BR to all ones. Check 		
005737		BR failed to set.	Display A to determine bit that failed. (failed bit $= 1.$)
005743	(b) Reset BR.	BR bit failed to reset.	Display A to determine bit that failed.
005747	(<i>c</i>) CLA IR1 in bank 001.	Wrong memory location read. (Should have read location 000000.)	Display A for address of location read.
005754	(d) CLA BRL 3 in bank 00.	Wrong memory location read. (Should have read location 0000007)	Display A for number of memory locations displaced.

Halt Location	Test Description	Test Result	Further Checks
	,		
005763	(e) Set BR to all ones. CLA IR1 in bank 77.	Wrong memory location read. (Should have read location 000770.)	Display A for number of memory locations
	(f) CLA BRL3 in bank 77.		
005770		Wrong memory location read. (Should have read location 000777.)	Display A for number of memory locations displaced.
	(g) STR a word containing 70705010 to IR1, bank 77. CLA location 000770. LGE with a word containing 00005010.		
006003 006004	·	Bit other an address written to IR1. Only sign bit and address written to IR1.	Display A for bit picked up.
	(<i>h</i>) STR a word containing 14500023 n BRL3 in bank 77. CLA location 00000777. LGE with a word containing 14500023.		
006017		Sign bit failed to clear.	Display A to determine if additional bits failed to clear
006020		Bit other than sign failed to clear.	Display A to determine bit that failed to clear.
	(7) <i>Register Transfer Checks.</i> (<i>a</i>) STR award containing 00077777 to SBR. Check results.		
006027		No ones transferred to SBR.	
006027		One or more bit failed.	Display A to determine bits that failed. (Failed bit = 1.)
	(<i>b</i>) STR a word containing all zeros to SBR. Check results.		
006037	(c) CLA the OAR, LGE was a word containing	Bit failed to clear in SBR.	Display A to determine bit that failed.
006042	03707777.	STP foiled during test (1) (b)	Display A to determine hit that failed
000043	(<i>d</i>) STR a word containing all zeros to OAR. LGM a word containing 7767777 with new contents of OAR.		Display A to determine bit that failed.
006051		Bit in OAR failed to clear.	Display A to determine bit that failed
	(e) CLA the PC. LGE a word confining 00006052 with PC.		
006055		PC transfer failed.	Display A to determine bit that failed.

Halt Location	Test Description	Test Result	Further Checks
	(<i>j</i>) STR a word containing 00077777 IAR. LGE a word containing 03707777 with new contents d IAR.		
006064		Bit picked up or dropped in STR to IAR.	Display A to determine bit failed.
006073	(g) STR a word containing all ones to LSR. LGE a word containing 01000077 with new contents of LSR.	Bit in IAR failed to clear.	Display A to determine bit that failed.
006102		Bit in LSR failed to set.	Display A to determine bit that failed. (failed bit $= 1$.)
006107	STR a word containing all zeros to LSR. Check. (8) <i>Indirect Addressing Check</i> .	Bit in LSR failed to clear.	Display A to determine bit that failed.
006113	 (9) Indexing Checks. (a) Clear BR. STR a word containing all ones to IR1, IR2, IR3 and IR4 in bank 00. CLA each index register and verify contents 	Indirect addressing failed.	
006174		Bit in IR1 failed to set.	Display A to determine hit that failed. (bit failed $=-1$)
006200		Bit in IR2 failed to set.	Display A to determine hit that failed. (bit failed -1)
006204		Bit in IR3 failed to set.	Display A to determine bit that failed. (bit failed -1)
006210		Bit in IR4 fail to set.	Display A to determine bit that failed. (bit failed $= 1.$)
	(<i>b</i>) STR a word containing all zeros to IR1, IR2, 1R3 and IR4 in bank 00. CLA each index register and verify contents		
006222 006226 006232 006236		Bit in IR1 failed to clear. Bit in IR2 failed to clear. Bit in IR3 failed to clear. Bit in IR4 failed to clear.	Display A to determine bit that failed. Display A to determine bit that failed. Display A to determine bit that failed. Display A to determine bit that failed.

Halt Location	Test Description	Test Result	Further Checks
006123	(<i>c</i>) Clear BR. STR a word containing all zeros in IR1 bank 00. CLA indexing unit IR1 bank 00.	Indexing failed.	Display A for number of memory locations displaced.
	(<i>d</i>) STR a word containing 00000001 to IR1 bank 00. Set BR to 77. STR a word containing all zeros to IR1 bank 77. CLA location 3771 indexed by IR1. LGE with location 3771 direct addresses (Location 003771 = 00000001).		
006135		Address indexed by wrong IR.	Exclusive OR contents of A with 00000001 to determine contents of memory location actually accessed.
	(a) STR a word containing all zeros to IR4. STR a word containing 00000001 to IR1. STR a word containing 0000002 to IR2. STR a word containing 00000003 to IR3. CLA location 3771 indexed by IR4.		
006153 006157 006158		Resulted in indexing by IR1, IR2 or IR3.	Exclusive OR contents of A with 00000002 to determine contents of memory location actually accessed.
	(10) <i>Index Register Store Checks.</i> STR a word of all ones to locations to assigned IR1, IR2, IR3, and IR4. After the contents of each index register with an STR to IR.		
006251	STR a word containing 00040000 to IR1. Check.	Bit(s) in IR1 failed to clear.	Display A for bit that failed. (failed bit = 1.)
006257	STR a word containing 00040001 to IR2. Check.	Bit(s) in IR2 failed to clear. Bit(s) in IR3 failed to clear	Display A for bit that failed. (failed bit = 1.) Display A for bits that failed. (failed bit = 1.)
006273	STR a word containing 00040002. It into: Check: (11) Index Register Access Checks. (a) CLA location 37740 (IR1), 37741 (IR2), 37742 (IR3) and 37743 (IR3) indexed by IR1	Bit(s) in IR4 failed to clear.	Display A for bit that failed. (failed bit = 1.)
006300		IR1 not accessed. IR1 = 00040000.)	Exclusive OR contents of A with 00040004 to determine contents of location actually accessed
006304		IR2 not accessed. (IR2 = 00040001.)	Exclusive OR contents of A with 0040001 to determine contents of location actively accessed.

Halt Location	Test Description	Test Result	Further Checks
006310		IR3 not accessed. (IR3 = 00040002.)	Exclusive OR contents of A with 00040002 to determine contents of location actually
006314		IR4 not accessed. (IR4 = 00040003.)	Exclusive OR contents of A with 00040003 to determine contents of location actually accessed.
	(<i>b</i>) CLA location 37140 (IR1) indexed by IR1, IR2,		
006320		IR1 not accessed.	Exclusive OR contents of A with 00040000 to determine contents of address actually accessed.
006324		IR2 not accessed.	Exclusive OR contents of A with 00040001 to determine contents of location actually accessed.
006352		IR3 not accessed.	Exclusive OR contents of A with 00040002 to determine contents of location actually
006334		IR4 not accessed.	Exclusive OR contents of A with 00040003 to determine contents of location actually accessed.
	 {12) Adders Checks (a) STR a word containing 00025252 to IR1. CLA to location 012525 indexed by IR1. Check. 		
006344		Failed to address location 077777.	Exclusive OR contents of A with 14500023 to determine contents of location actually accessed.
	(b) STR a word containing 00012525 to IR1. CLA		
006352	to location 025252 indexed by IR1. Check.	Failed to address location 077777.	Exclusive OR contents of A with 14500013 to determine contents of location actually
			accessed.
006360	(c) CLA location 012525 indexed by IR1.	Failed to address location 025252.	Exclusive OR contents of A with 00400000 to determine contents of location actually accessed.
	(d) STR a word containing 0015252 to IR1. CLA to		
006370	location 15252 indexed by IRT.	Failed address location 032524.	Exclusive OR contents of A with 145000213 to determine contents of location actually accessed.
	(e) Set BR to 77. STR a word containing 00077777 to IR1. CLA location 000001 indexed by IR1.		

Halt Location	Test Description	Test Result	Further Checks
006402		Failed to address location 000000.	Exclusive OR contents of A with 00400000 to determine contents of location actually
006410	(<i>f</i>) STR a word containing 00000001 to IR4. CLA location 06401 indexed by IR4 with indirect addressing.	Failed to address location 06377.	Exclusive OR contents of A with 55400001 to determine contents of location actually accessed.
	(13) <i>EOAX Register Checks.</i> (a) STR a word containing 00006414 to PEX.		
006413	(b) I GM a word containing 00300000 wit PCS	STR to PEX failed.	Display PEX to determine bit that failed.
006417		EOAX bits not reset.	
006422		PC transfer failed.	
006426	(d) LGE the PEX with a word containing 00106423.	EOAX bit 1 failed to set.	
006431	(e) STR 00206432 to PEX.	PC transfer failed.	
	(7) LGE the PEX with a word containing 002006432.		
006435	(g) STR 00306441 to PEX.	EOAX bit 2 failed to set.	
006440	(<i>b</i>) LGE the PEX with a word containing 00306441.	PC transfer failed.	
006444	()	EOAX bit 1 or 2 failed to set.	Display A to determine bit that failed (failed bit -1)
000447 006460	 (<i>i</i>) STR 00006450 to PEX. (14) <i>Indirect Addressing Checks.</i> (<i>a</i>) STR a word containing 22006506 in location 	PC transfer failed. PC overflow failed.	- 1).
	 37703 page 1. Using indirect addressing, STR a word containing 22006510 in location. 37704 page 1 using indirect addressing. (<i>b</i>) CLA location 37703 page 2 using indirect addressing. 		
Halt Location	Test Description	Test Result	Further Checks
----------------------	--	--	---
006476		Indirect addressing failed.	Display A for contents of location actually accessed.
006503	(<i>c</i>) CLA location 33704 page 2 using indirect addressing.	Indirect addressing failed.	Display A for contents of location actually
006505	(<i>d</i>) TRU to location 37703 page 1. (<i>e</i>) TRU to location 37704 page 2.	Indirect transfer to page 1 failed.	
006507	(f) CLA location 000000 using indirect indexed	Indirect transfer to page 1 failed.	
006514	addressing.	Indirect Indexing failed.	Display A for contents of location actually accessed.
	(<i>g</i>) STR 00007777 to IR4. STR 00100000 to location-020000. STR 22000305 to location 00160000 using Indirect addressing. TRU to location 020000 using indexed addressing.	TRU indexed indirect failed.	
	(<i>h</i>) STR a word in location 020000 page 0. CLA a word from location 020000 with page bit (bit 09) set		
006535	301.	Failed to access location 020000 page 0.	Exclusive OR contents of A with 22000532 to determine contents of location actually accessed.
006545	(<i>i</i>) STR to location 020000 page 0. CL.A to location 020000 page 2 with page bit (bit 09) = 0.	Page bit control failed.	Exclusive OR contents of A with 00277704 to determine contents of location actually accessed
006547	End of test.		
<u>d</u> . Miscellar	neous Halts.		
Halt Location	Test Description	Test Result	Further Checks
	(1) <i>Memory Error Halts.</i> The following halts should not be encountered during the bootstrap and memory off-line diagnostic test.		

Halt Location	Test Description	Test Result	Further Checks
005700		This halt can be encountered only as a result of attempts to continue testing after a BC740 or BC750 halt.	REDO BASIC MEM is printed.
005714		This halt can be encountered only as a result of attempts to continue testing after one or more BC680 or BC710 halts.	CALL IN MAIN MEM TEST is printed.
005713		Incorrect status received from local page printer when attempting BC740 printout.	
005730		This halt can be encountered only as a result of attempts to continue testing after one or more BC680 or BC710 balts	CALL IN MAIN MEM TEST is printed.
005727		Incorrect status received from local page printer when attempting BC750 printout.	
077700	(2) Transfer Error Halts.		
377700		I RN occurred with $A = 00000000$.	
377702		TRP occurred with $A = 7777777$	
311102	(3) Print Routine Halts		
006607	Read status and set BB.		
006617	Write character.		
006621	Read status.		
006666	Write status.		

EXHIBIT H

MEMORY-TO-MEMORY DIAGNOSTIC PROGRAM

Section I. GENERAL

The Memory-to-Memory diagnostic program is used to test the logic circuits and functions associated with the transfer of information from one processor to the other and to verify the proper operation of the control transfer logic. The particular tests in the Memory-to-Memory diagnostic program proceed along a path of increasing usage of mechanization and logic associated with the memory-to-memory transfer operation which is the receipt and transmission of data and status information between processors.

The diagnostic program consists of two sections; one of

which is loaded into the "transmitting processor" and the other section is loaded into the "receiving processor." The "transmitting processor" contains the interrupt processor routine, the teletype print routine, the memory-to-memory test routine, the transfer control routine, and the idle routine. The "receiving processor" contains routines to read the data transmitted by the active processor routines to return the data, control transfer interface routines, an interrupt processor control routine and an error printout routine.

Section II. DIAGNOSTIC PROGRAM

THE FOLLOWING PROCEDURES ARE USED TO CONVERT THE OPERATIONAL PRELOADER PROGRAM TO THE OFF-LINE DIAGNOSTIC PRELOADER PROGRAM

- 1. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 2. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 3. Set the WSR toggle switches to 00277750.
- Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A. 5. Set the WSR toggle switches to 55137754. 6.
- 7. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified on the on-line program preloader instruction entries chart below. If the entries do not agree, or are absent, the on-line program preloader instructions must be loaded into memory before proceeding. If the entries appearing in parenthesis on the chart are already loaded into memory, proceed to step 42 below.
- Set the MEMORY guarded switch to the UNPROTECTED position. 8.
- 9. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 10. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 11. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 12. Verify that the CLOCK OPERATE CONTROL rotary switch is in the CONT position.
- 13. Press the CLEAR pushbutton switch.
- 14. Set the WSR toggle switches to 00277750.

- 15. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 16. Set the OPERATIONAL CONTROL rotary switch to STORE SEQ1 and the REGISTER SELECT to MEM.
- 17. Set the WSR toggle switches to the instruction entries listed in the on-line preloader instruction chart and press the INITIATE pushbutton switch after each setting. Observe that the BUS INDICATOR displays the entered instruction.
- 18. Press NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator lights.
- 19. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 20. Set the WSR toggle switches to 00277750.
- 21. Press the INITIATE pushbutton switch and observe that BUS INDICATOR displays the address listed.

Preloader Instructions Chart

Address	Instruction
00277750	01077751
00277751	00002404
00277752	05200377
00277753	24077755
00277754	22077750
00277755	70100000
00277756	7000001
00277757	01077760
00277760	00002400
00277761	02000040
00277762	24077757
00277763	01077764
00277764	00002404
00277765	34000020
00277766	35000010
00277767	7200001
00277770	7400003
00277771	22077757
00277772	62501776 (62500476)
00277773	72100001
00277774	74100107 (74100235)
00277775	22077756
00277776	0000000

- 22. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A.
- 23. Set the WSR toggle switches to 55137754.
- 24. Press INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified on the chart.

NOTE

The following procedures will correct an erroneous address entered from the chart of specified addresses and instructions.

- a. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- b. Set the ASR toggle switches to the correct address.
- c. Press INITIATE pushbutton switch and observe that the BUS INDICATOR displays the correct address.
- *d.* Set the WSR toggle switches to the *correct instruction number*.
- e. Set the OPERATIONAL CONTROL rotary switch to STORE.
- f. Press INITIATE pushbutton switch and observe BUS INDICATOR displays the correct instruction.

- g. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- h. Press INITIATE pushbutton switch and verify that the BUS INDICATOR displays the correct instruction.
- 25. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 26. Set the MEMORY guarded switch to the UNPROTECTED position.
- 27. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- 28. Set the ASR toggle switches to 277772.
- 29. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62501776.
- 30. Set the WSR toggle switches to 62400476.
- 31. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 32. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62500476.
- 33. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 34. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62500476.
- 35. Set the ASR toggle switches to 277774.
- 36. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100107.
- 37. Set the WSR toggle switches to 74100235.
- 38. Set the OPERATIONAL CONTROL rotary switch and observe that the BUS INDICATOR displays a reading of 74100235.
- 40. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 41. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100235.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE OFF-LINE DIAGNOSTIC LOADER PROGRAM INTO MEMORY

- 42. Load the off-line diagnostic loader tape (SM-D-752126) on the paper tape reader.
- 43. Set the paper tape reader MODE SELECT toggle switch to STRIP and the PWR switch to ON.
- 44. Set the system status panel RESET SELECT TAPE READER toggle switch to ON.
- 45. Press the system status panel RESET pushbutton switch several times and observe that the loader tape moves.
- 46. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT Indicator illuminates.
- 47. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 48. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 49. Set the WSR toggle switches to 00277750.
- 50. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 51. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 52. Set the RUN/ONE INSTR toggle switch to RUN.
- 53. Press the INITIATE pushbutton switch an observe that:
 - a. Off-line diagnostic loader tape strip loads into memory.
 - b. PRGM HALT indicator illuminates at the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00277777.
- 54. Rewind the loader tape by setting the system status panel TAPE READER REWIND toggle switch to ON.

NOTE

The procedures outlined in steps 1 through 54 above must be repeated on the other processor, using the other Maintenance Control Panel.

- 65. Set the PARITY ERROR HALT toggle switch to OFF.
- 56. Set the CLOCK OPERATE CONTROL rotary switch to CONT.
- 57. Set the ADV-RPT toggle switch to ADV.
- 58. Set the REAL TIME CLOCK guarded switch to the DISABLE position.
- 59. Verify that the REGISTER SELECT rotary switch is set to PEX.
- 60. Set the CONTROL TRANSFER toggle switch to DISABLE.
- 61. Set the printer motor control BYPASS toggle switch to BYPASS.
- 62. Set the MEMORY guarded switch to the PROTECTED position.

THE FOLLOWING PROCEDURES LOAD THE DIAGNOSTIC PROGRAM INTO MEMORY

- 63. Load the Memory (SM-D-751716) and Memory-to-Memory and Control XFR (SM-D-751717) diagnostic program tapes on the paper tape reader.
- 64. Set the paper tape reader MODE SELECT toggle switch to REEL and the PWR switch to ON.
- 65. Press the NORMAL HALT pushbutton switch and observe that the PRGM HALT indicator extinguishes and the PRCS HALT indicator illuminates.
- 66. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 67. Set the WSR toggle switches to 00000500.
- 68. Press the INITIATE pushbutton switch and observe the BUS INDICATOR displays a reading of 00000600.
- 69. Press the system status panel RESET pushbutton switch and observe that the diagnostic tape moves.
- 70. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 71. Set the RUN/ONE INSTR toggle switch to RUN.
- 72. Press the INITIATE pushbutton switch and observe that:
 - a. Diagnostic tape begins to load into memory.
 - b. PRGM HALT indicator illuminates.
 - c. BUS INDICATOR displays a reading of 0000631.
- 73. Press the INITIATE pushbutton switch twice more to load-in all three segments of the Memory-to-Memory diagnostic program and observe that the same indications observed in step 72 above are obtained.
- 74. Repeat the procedures outlined in steps 63 through 73 above on the other processor, using the other Maintenance Control Panel.

THE FOLLOWING PROCEDURES ARE USED TO SELECT THE TRANSMITTING (PROCESSOR A) AND THE RECEIVING PROCESSOR (PROCESSOR B)

- 75. Set the REGISTER SELECT rotary switch to CPS on both processors.
 - a. If the desired processor to be selected as the transmitting processor has its CPS Bit 23 set (BUS INDICATOR bit 23 is illuminated), press the CONTROL TRANSFER MANUAL pushbutton switch twice and observe that the BUS INDICATOR bit extinguishes and then illuminates.
 - b. If the desired processor to be selected as the transmitting processor (processor A) does not have is CPS bit 23 set (BUS INDICATOR bit 23 is illuminated), press the CONTROL TRANSFER MANUAL pushbutton switch three times and observe that the bit illuminates, extinguishes, and then illuminates again.

NOTE

By pressing the CONTROL TRANSFER MANUAL pushbutton more than once it verifies that the transfer tree is in its initial state. The reader Is cautioned to remember which processor is "A" (CPS bit 23-1) and which processor is "B" (CPS bit 23-0) throughout the remainder of the test.

THE FOLLOWING PROCEDURES ARE USED TO START THE OFF-LINE DIAGNOSTIC PROGRAM

- 76. Set both REGISTER SELECT rotary switches to PEX.
- 77. Press both NORMAL HALT pushbutton switches and observe that both PRGM HALT indicators illuminate.
- 78. Press both CLEAR pushbutton switches.
- 79. Set both OPERATIONAL CONTROL rotary switches to STORE.
- 80. Set the WSR toggle switches to 00010000 on the transmit processor (A) and to 00015600 on the receive processor (B).
- 81. Press the INITIATE pushbutton switch on transmit processor (A) and observe that the BUS INDICATOR displays a reading of 00010000.
- 82. Press the INITIATE pushbutton switch on receive processor (B) and observe that BUS INDICATOR displays a reading of 00015000.
- 83. Set the system status panel RESET SELECT LOCAL PRINTER toggle switch to ON and press the RESET pushbutton switch.
- 84. Set the WSR toggle switches to all zeros on both panels.
- 85. Set both OPERATIONAL CONTROL rotary switches to CMPT.
- 86. Set the system status panel RESET SELECT MEM/MEM toggle switch to ON and press the RESET pushbutton several times.
- 87. Press the INITIATE pushbutton switch on both processors and observe that:
 - a. Both PRGM HALT Indicators illuminate.
 - b. Transmit processor (A) BUS INDICATOR displays a reading of 00010015.
 - c. Receive processor (B) BUS INDICATOR displays a reading of 00015015.
 - d. MM TEST PROCA message is generated on page printer from transmit processor.
 - e. REC CP RDY message is generated on page printer from receiving processor.
- 88. To successfully execute the following procedure, the specified actions must be performed within 5 seconds of the PRGM HALT indicator illuminating with the stated BUS INDICATOR displays.

BUS INDICATOR	Operator action	Processor action
00010015	Press INITIATE pushbutton on (A).	Starts test.
00015015	Press INITIATE pushbutton on (B).	Starts test.
0000017	Set CONTROL TRANSFER AUTO toggle switch to ENABLE.	Control transfer to (B) and then back to (A).
00000022	Set CONTROL TRANSFER AUTO toggle switch to DISABLE and	Control transfers to (B).
	press CONTROL TRANSFER MANUAL pushbutton switch.	
0000023	Press CONTROL TRANSFER MANUAL pushbutton switch.	Control transfers to (A).

89. Observe that both PRGM HALT Indicators illuminate and the transmitting processor (A) BUS INDICATOR displays a reading of 00013300 and the receiver processor (B) BUS INDICATOR displays 00016251.

Section III. ERROR PRINTOUTS

		Error		Logic	
5.4.4	-	vector	_	associated	Suggested further
Printout	lest description	<u>XX</u> =	Error	with failure	checks and remarks
1. CT01- <u>XX</u>	Instruction: (Processor A)	01	CPS 08 failed to reset.		
	SL1				
	STR (CPS)	00	000 44 5 5 5		
	Logic tested: (Processor A)	02	CPS 11 is set.		Should be set only when control
	CPS register				transfer is in progress.
	Initial conditions:	03	CPS 22 not set.		Check CPS 08 in processor B.
	(Processor A)				CPS22 is reflection of CPS
	(A) = 00000000				in alternate processor.
	CONTROL TRANSFER AUTO set to DISABLE	04	CPS 23 not set.		
	Correct answer:				
	(Processor A)				
2 CT04-XX	Instruction: (Processor A)	01	Interrupt failed to occur		
2. 0101 /04	STR (CPS)	01			
	Logic tested: (Processor A)	02	CPS 11 failed to reset after interrupt.		
	Interrupt logic				
	CPS register	03	CPS 23 reset as a result of interrupt.		
	UPS register				
	(Processor A)				
	CPS 08 = 0				
	CPS 08 = 0				
	CONTROL TRANSFER AUTO set to DISABLE				
	Correct answer:				
	Interrupt occurs and program Interrupt routine				
3 CT01-XX	Instruction: (Processor A)	01	CPA 08 failed to reset		
0. 0101 <u>////</u>	SL1	Ŭ,			
	STR (CPS)				
	Logic tested: (Processor A)	02	CPS 11 is set.		Should be set only when control
	KL counter	00			transfer is in progress.
	UPS register	03	CPS 22 not set		Chack CBS 08 in processor B
	(A) = 00000000	04	GF 3 23 Hot Set.		CPS22 is reflection of CPS 98 in
	CONTROL TRANSFER AUTO set to DISABLE				alternate processor.
	Correct answer:				·
	(Processor A) (CPS) = 00000003				
4. CT04- <u>XX</u>	Instruction: (Processor A) STR (CPS)	01	Interrupt failed to occur.		
	Logic tested: (Processor A)	02	CPS 11 failed to reset after interrupt.		
	Interrupt logic				

Printout	Test description	Error vector <u>XX</u> =	Error	Logic associated with failure	Suggested further checks and remarks
C C Initia (F C C C C C C C C C C C C C C C C C C	PS register PD register al conditions: Processor A) PS 08 = 0 PD 08 = 0 NTROL TRANSFER AUTO set to DISABLE rect answer: terrupt occurs and program interrupt routine is ntered.	03	CPS 23 reset as a result of interrupt.		

Section IV. TROUBLESHOOTING CHART

Malfunction	Probable cause	Corrective action
MMDR-01 (reported by Processor B)	Data received by processor B differs from data expected. Data expected was 377, 252, 125 and 000 in that order.	Replace following cards in sequence. Repeat test after each replacement. (1) MOS3 (2) MOS1
MMDR-76 (reported by Processor B)	Processor A failed to send character	Replace MOS2 card. Repeat test.
MMMT14-XX	Attempt to send a block of data containing 22 transmissions of 377, 252, 125 and 00. How processor A to processor B failed.	Refer to <u>XX</u> condition.
<i>a.</i> Where <u>XX</u> is 74 or 75.	 Processor B failed to accept data. 	a. Replace MOS2 card. Repeat test.
<i>b.</i> Where <u>XX</u> is 76.	b. Processor B failed to return data.	b. Replace MOS2 card. Repeat test.
<i>c.</i> Where <u>XX</u> is 77.	 Data returned from processor B differs from data sent by processor A. 	 c. Replace following cards in sequence. Repeat test after each replacement. (1) MOS3 (2) MOS1
MMBL-XX (reported by Processor B)	Attempt by processor B to receive and return a block of data containing 22 transmissions of 377, 252, 125 and 000 failed.	Refer to <u>XX</u> condition.
a. Where <u>XX</u> is 74.	 Processor A did not accept returned data. 	a. Replace MOS2 card. Repeat test.
 b. Where <u>XX</u> is 76. c. Where <u>XX</u> is 77. 	 b. Processor A failed to send data. c. Data received by processor B differs from data expected. 	 b. Replace MOS2 card. Repeat test. c. Replace following cards in sequence. Repeat test after each replacement. (1) MOS3 (2) MOS1
While running control transfer test, any of following printouts may occur prior to END OF CLT XFR TEST printout.		NOTE Cards located in syn- chronizer A16.
 a. CT01-XX where XX is 01 through 04. 	 a. Processor A control transfer logic defective. 	 Refer malfunction to higher category maintenance.
b. CT01-05	b. Alarm register circuits defective.	 b. Replace following system alarm cards in sequence. Repeat test after each replacement. (1) Remove I/O inhibit alarm. (a) Alarm latch. (b) Alarm gate. (c) Bus drivers. (2) Line load set alarm. (a) Alarm latch. (b) Alarm gate. (c) Bus drivers.
 CT02-<u>XX</u> where <u>XX</u> is 01 through 05. 	 Control transfer logic processor A failed during automatic control transfer processor A to processor B. 	 c. Replace following cards in sequence. Repeat test after each replacement. (1) A224 (2) A221 (3) A223 (4) A222 (5) A220
d. CR02-06	d. Alarm register	 Replace following Remote I/O inhibit alarm cards in sequence. Repeat test after each replacement. (1) Alarm latch (2) Alarm cata

(2) Alarm gate(3) Bus drivers.

	Malfunction		Probable cause		Corrective action
e.	CT03- <u>XX</u> where <u>XX</u> is 06, 07, or 10.	e.	Control transfer logic. Processor A failed during automatic control transfer processor B to processor A.	e.	 Replace following cards in sequence. Repeat test after each replacement. (1) A224 (2) A221 (3) A223 (4) A222 (5) A220
f.	CT03-11	f.	Alarm register.	f.	 (3) A220 Replace following system alarm cards in sequence. Repeat test after each replacement. (1) Line load set alarm. (a) Alarm latch (b) Alarm gate. (c) Bus drivers.
					 (2) Remote I/O inhibit alarm. (a) Alarm latch (b) Alarm gate. (c) Bus drivers. (3) Spare alarm (a) A247 (b) A248 (c) A249
g.	CT04- <u>XX</u> where <u>XX</u> is 01 through	g.	Processor A control transfer	g.	(<i>d</i>) A250 Refer malfunction to higher category
h.	03. CT04, 04	h.	logic. Alarm register.	h.	maintenance. Replace following system alarm cards in sequence. Repeat test after each
					replacement. (1) Spare alarm. (a) A247 (b) A248 (c) A249 (d) A250 (2) Remote I/O inhibit alarm. (a) Alarm latch (b) Alarm gate (c) Bus drivers (3) Line load set alarm
					 (a) Alarm latch (b) Alarm gate (c) Bus drivers
i.	CT04, 77	i.	Automatic control transfer inhibit logic processor A.	i.	Replace A222 card. Repeat test.
j.	CT-5- <u>XX</u> where <u>XX</u> is 01 through 04.	j.	Control transfer logic Processor A failed during manual control transfer processor A to processor B.	j.	 Replace following cards in sequence. Repeat test after each replacement. (1) A224 (2) A221 (3) A223 (4) A222 (5) A220
k.	CT05-05	h.	Alarm register.	k.	 Replace following system alarm cards in sequence. Repeat test after each replacement. (1) Line load set alarm. (a) Alarm latch. (b) Alarm gate. (c) Bus driver. (2) Remote I/O inhibit alarm. (a) Alarm latch
					 (b) Alarm gate (c) Bus driver (3) Spare alarm (a) A247

Malfunction Probable cause					Corrective action
					(b) A248
					(<i>c</i>) A249
I.	CT06- <u>XX</u> where <u>XX</u> is 06, 07, or 10.	I.	Control transfer logic. Processor A failed during manual control transfer processor B to processor A.	I.	 (d) A250 Replace following cards in sequence. Repeat test after each replacement. (1) A224 (2) A221 (3) A223
m.	CT06-11	m.	Alarm register.	m.	(4) A222(5) A220Replace following system alarm cards
			J		 in sequence. Repeat test after each replacement. (1) Remote I/O inhibit alarm. (a) Alarm latch (b) Alarm gate (c) Bus driver (2) Spare alarm (a) A247 (b) A248 (c) A249 (d) A250
n.	CT07- <u>XX</u> where <u>XX</u> is 70 or 71. This printout occurs only when WORD SWITCH REGISTER bit 3 option is selected.	n.	Control transfer logic processor A.	n.	Replace following cards in sequence. Repeat test after each replacement. (1) A224 (2) A221 (3) A223 (4) A222 (5) A220
о.	MMAC- <u>XX</u> (reported by processor B where <u>XX</u> is 07, 10 or 11.	0.	Control transfer logic processor B during automatic control transfer processor A to processor B.	о.	 Replace following cards in sequence. Repeat test after each replacement. (1) A224 (2) A221 (3) A223 (4) A222 (5) A220
<i>p.</i>	MMAC-12 (reported by processor B.	p.	Alarm register.	p.	 Replace following remote I/O inhibit alarm cards in sequence. Repeat test after each replacement. (1) Alarm latch (2) Alarm gate (3) Bus drivers.
q.	MMAC- <u>XX</u> (reported by processor B) where <u>XX</u> is 13 through 15.	q.	Automatic control transfer inhibit logic processor B.	q.	Réplace A222. Repeat test.
r.	MMAC-16 (reported by processor B).	r.	Alarm register.	r.	Replace following remote I/O inhibit alarm cards. Repeat test after each replacement. (1) Alarm latch (2) Alarm gate (3) Bus drivers
S.	MMRC- <u>XX</u> (reported by processor B) where <u>XX</u> is 01 through 05.	S.	Control transfer logic processor B during automatic control transfer processor B to processor A.	S.	 Replace following cards in sequence. Repeat test after each replacement. (1) A224 (2) A221 (3) A223 (4) A222 (5) A220
t.	MMRC-06	t.	Alarm register.	t.	Replace following system alarm cards sequence. Repeat test after each replacement.

Malfunction Probable cause				Corrective action				
					 (1) Line load set alarm. (a) Alarm latch (b) Alarm gate (c) Bus drivers 			
					 (c) Bas diversion (c) Parameters (a) Alarm latch (b) Alarm gate (c) Bus drivers (3) Spare alarm (a) A247 (b) A248 (c) A249 			
u.	MMC- <u>XX</u> (reported by processor B) where <u>XX</u> is 06, 07 0r 10.	u.	Control transfer logic processor B during manual control transfer processor A to processor B.	u.	 (d) A250 Replace following cards in sequence. Repent test after each replacement. (1) A224. (2) A221 (3) A223 (4) A222 			
v.	MMC-11 (reported by processor B).	V.	Alarm register.	V.	 (4) A222 Replace following system alarm cards in sequence. Repeat test after each replacement. (1) Line load set alarm. (a) Alarm latch (b) Alarm gate (c) Bus drivers (2) Remote I/O inhibit alarm. (a) Alarm latch (b) Alarm gate (c) Bus drivers. (3) Spare alarm. (a) A247 (b) A248 (c) A249 (d) A250 			
W.	MMRM- <u>XX</u> (reported by processor B) where <u>XX</u> is 01 through 04.	W.	Control transfer logic processor B during manual control transfer processor B to processor A.	w.	 Replace following cards in sequence. Repeat test after each replacement. (1) A224. (2) A221 (3) A223 (4) A222 (5) A220 			
Х.	MMRM-05 (reported by processor B).	Х.	Alarm register.	Х.	 Replace following system alarm cards in sequence. Repeat test after each replacement. (1) Remote I/O inhibit alarm. (a) Alarm latch (b) Alarm gate (c) Bus drivers (2) Spare alarm. (a) A247 (b) A248 (c) A249 (d) A250 			
у.	MMAT-XX (reported by processor B) where XX is 70 or 71. This printout occurs only when WORD SWITCH REGISTER bit 3 option is selected.	у.	Control transfer logic processor B.	у.	 Replace following cards in sequence. Repeat test after each replacement. (1) A224 (2) A221 (3) A223 (4) A222 (5) A220 			

EXHIBIT I

PAPER TAPE READER/PAPER TAPE PUNCH DIAGNOSTIC PROGRAM

Section I. GENERAL

This diagnostic program is used whenever data transfer problems are encountered with the Paper Tape Reader (PTR) or Paper Tape Punch (PTP) and is designed to check the functional operation of the processor-synchronizer and device synchronizer interface. The PRP/PTR diagnostic program is divided into manual and programmed tests. Since the testing of the Paper Tape Reader require paper punch test tapes, it is required that the paper tape punch portion of the diagnostic program be executed first.

The WSR toggle switch bit positions control the sequence of tests executed for the Paper Tape Reader and indicate the format of the data to be processed. The program reads the paper tape and examines each character read for validity and the timing of the data transfer is monitored to ensure the timing is within tolerance.

There are three (3) paper tape formats which are processed: Octal, ASCII, and Constant Value. If the Octal character is selected, the program generates 10 blocks of 100 characters each for a total of 1,000 characters. The block consists of the following data:

Block Number	Data
1	0
2	1
3	2
4	4
5	10
6	20
7	40
8	100
9	200
10	377

If the ASCII character is selected, the program generates 10 blocks of 128 characters. The 128 characters represent all possible combinations for ASCII. The characters are also displayed on the local page printer one block at a time. The tape can be prematurely terminated by setting the WSR toggle switch bit 13 to a 1. The ASCII character tape is used when executing the Paper Tape Reader test.

If the constant character is selected, WSR toggle switch bits 16 through 23 should specify the particular character. The program generates 100 characters per block and 25 blocks for a total of 2,500 characters before terminating by itself. The constant character tape is used in the timing section of the Paper Tape Reader test. To terminate prematurely, WSR toggle switch bit 13 should be set to a 1; the program will terminate after it has completed the block of 100 characters that it is presently processing.

A summary of the various formats is contained in the following chart:

	WSR Bits										
Format	13	14	15	16	17	18	19	20	21	22	23
Constant Character		1	0		(1	Data fo	or Con	stant C	haract	er)	
ASCII		Ō	1								
Octal		0	0								
Invalid		1	1								
Terminate	1										

Section II. DIAGNOSTIC PROGRAM

- 1. Set the MEMORY guarded switch to the PROTECTED position.
- 2. Set the PARITY ERROR HALT toggle switch to OFF.
- 3. Set the CLOCK OPERATE CONTROL rotary switch to CONT.
- 4. Set the ADV-RPT toggle switch to ADV.
- 5. Set the REAL TIME CLOCK guarded switch to the DISABLE position.
- 6. Set the CONTROL TRANSFER toggle switch to DISABLE.
- 7. Set the printer motor control BYPASS toggle switch to BYPASS.

THE FOLLOWING PROCEDURES LOAD THE TABLE OF INSTRUCTIONS FOR EXERCISING THE PTP

- 8. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 9. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 10. Press the CLEAR pushbutton switch.
- 11. Set the WSR toggle switches to 00000776.
- 12. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- 13. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00000776.
- 14. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 15. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00000776.
- 16. Set the OPERATIONAL CONTROL rotary switch to STORE SEQL and the REGISTER SELECT to MEM.
- 17. Set the WSR toggle switches to each of the instruction entries listed below and press the INITIATE pushbutton switch after each setting. Observe that the BUS INDICATOR displays the entered instruction.

Address	Instructions
00000776	01200420
00000777	0000000
00001000	01001001
00001001	00000400
00001002	05200020
00001003	24001005
00001004	22001000
00001005	55200XXX
00001006	60037757
00001007	01001010
00001010	00000414
00001011	22001000

NOTE

XXX is the octal equivalent of the character to be repeatedly punched on the test; e.g., XXX would be 125 for a 01, 010, 101 punched character pattern or 252 for a 10, 101,010 punched character pattern.

- 18. Press NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 19. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX. Observe that the BUS INDICATOR displays a reading of 00001012.
- 20. Set the WSR toggle switches to 00000776.
- 21. Press the INITIATE pushbutton switch and observe that BUS INDICATOR displays a reading of 00000776.

- 22. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A.
- 23. Set the WSR toggle switches to 56137754.
- 24. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified in step 17 above.

NOTE

The following procedures will correct an erroneous address entered from the chart of specified addresses and instructions.

- a. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY the REGISTER SELECT to MEM.
- b. Set the ASR toggle switches t the correct address.
- c. Press INITIATE pushbutton switch and observe that the BUS INDICATOR displays the correct address.
- d. Set the WSR toggle switches to the correct instruction number.
- e. Set the OPERATIONAL CONTROL rotary switch to STORE.
- f. Press INITIATE pushbutton switch and observe BUS INDICATOR displays the correct instruction.
- g. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- *h*. Press INITIATE pushbutton switch and verify that the BUS INDICATOR displays the correct instruction.
- 25. Set the system status panel RESET SELECT TAPE PUNCH and TAPE READER toggle switches to ON.
- 26. Press the system status panel RESET pushbutton switch several times.

THE FOLLOWING PROCEDURES ARE USED TO OBTAIN A LEADER ON THE PTP

- 27. Press the paper tape punch OFF pushbutton switch.
- 28. Set the LINE-OFF-LOCAL rotary switch to OFF.
- 29. Press the paper tape punch ON pushbutton switch and obtain approximately 1/2 foot leader.
- 30. Press the paper tape punch OFF pushbutton switch.
- 31. Set the LIN-OFF-LOCAL rotary switch to LINE.
- 32. Press the Paper tape punch ON pushbutton switch.
- Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX. Observe that the BUS INDICATOR displays a reading of 00001012.
- 34. Set the WSR toggle switches to 00000776.
- 35. Press the INITIATE pushbutton switch and observe the BUS INDICATOR displays a reading of 0000076.
- 36. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 37. Set the RUN/ONE INSTR toggle switch to RUN.
- 38. Press the INITIATE pushbutton switch and observe that the paper taps punch starts to generate a tape of selected characters.
- 39. Visually inspect the punched tape for the correct format:

Tape								Character			
0	0	0	0	0.	0	0	0	377			
0		0	0		0	0		266			
	0	0		0.	0		0	155			
		0			0			044			

- 40. After a sufficient amount of punched tape has been generated, press the NORMAL HALT pushbutton switch and observe that the PRCS HALT Indicator illuminates.
- 41. Load the paper tape (step 40 above) on the paper tape reader.

NOTE

The data portion (punched holes) must be under the read head for starting the test.

- 42. Set the paper tape reader MODE SELECT toggle switch to STRIP and the PWR switch to ON.
- 43. Press the system status panel RESET pushbutton switch several times and observe that the paper tape moves.
- 44. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT Indicator illuminates.
- 45. Press the CLEAR pushbutton switch.
- 46. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 47 Set the WSR toggle switches to 00002000.
- 48. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 49. Press the INITIATE pushbutton switch and observe that BUS INDICATOR displays a reading of 00002000.
- 50. Set the OPERATIONAL CONTROL rotary switch to STORE SEQL and the REGISTER SELECT to MEM.
- 51. Set WSR toggle switches to the instruction entries listed below and press the INITIATE pushbutton switch after each setting. Observe that the BUS INDICATOR displays the entered instruction.

Address	Instruction
002000	01002001
002001	00002400
002002	02200040
002003	24002000
002004	01002005
001005	00002404
002006	60027757
002007	05200XXX
002010	24002000
002011	00002000
002012	22002000

NOTE

XXX is the octal equivalent of the constant character punched on the test tape.

- 52. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 53. Set the WSR toggle switches to 00002000.
- 54. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00002000.
- 55. Set the RUN/ONE INSTR toggle switch to RUN.
- 56. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 57. Press the INITIATE pushbutton switch and observe that:
 - a. Test tape reads into memory.
 - b. PRGM HALT indicator illuminates.
 - c. BUS INDICATOR displays a reading of 00002012.
- 58. Set the REGISTER SELECT rotary switch to position A and observe that the BUS INDICATOR displays whatever data entered in XXX.

THE FOLLOWING PROCEDURES ARE USED TO CONVERT THE OPERATIONAL PRELOADER PROGRAM TO THE OFF-LINE DIAGNOSTIC PRELOADER PROGRAM

- 59. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 60. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.

- 61. Set the WSR toggle switches to 00277750.
- 62. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 63. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A.
- 64. Set the WSR toggle switches to 55137754.
- 65. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified on the on-line program preloader instruction entries chart below. If the entries do not agree, or are absent, the on-line program preloader instructions *must be loaded into memory before proceeding*. If the entries appearing in parenthesis on the chart are already loaded into memory, proceed to step 100 below.
- 66. Set the MEMORY guarded switch to the UNPROTECTED position.
- 67. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT Indicator illuminates.
- 68. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 69. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 70. Verify that the CLOCK OPERATE CONTROL rotary switch is in the CONT position.
- 71. Press the CLEAR pushbutton switch.
- 72. Set the WSR toggle switches to 00277750.
- 73. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 74. Set the OPERATIONAL CONTROL rotary switch to STORE SEQL and the REGISTER SELECT to MEM.

Address	Instruction
00277750	01077751
00277751	00002404
00277752	05200377
00277753	24077755
00277754	22077750
00277755	70100000
00277756	7000001
00277757	01077760
00277760	00002400
00277761	00002400
00277761	00200040
00277762	24077757
00277763	01077764
00277764	00002404
00277765	34000020
00277766	35000010
00277767	7200001
00277770	7400003
00277771	220777571
00277772	62501776 (62500476)
00277773	72100001
00277774	74100107 (74100236)
00277775	22077756
00277776	0000000

75. Set the WSR toggle switches to the instruction entries listed in the on-line preloader instruction chart and press the INITIATE pushbutton switch after each setting. Observe that the BUS INDICATOR displays the entered instruction.

76. Press the NORMAL HALT pushbutton switch an observe that the PRCS HALT indicator lights.

77. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.

- 78. Set the WSR toggle switches to 00277750.
- 79. Press the INITIATE pushbutton switch and observe that BUS INDICATOR displays the address listed.
- 80. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A.
- 81. Set the WSR toggle switches to 55137754.
- 82. Press INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified on the chart.

NOTE

The following procedures will correct an erroneous address entered from the chart of specified addresses and instructions.

- a. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- b. Set the ASR toggle switches to the correct address.
- c. Press INITIATE pushbutton switch and observe that the BUS INDICATOR displays the correct address.
- d. Set the WSR toggle switches to the correct instruction number.
- e. Set the OPERATIONAL CONTROL rotary switch to STORE.
- f. Press INITIATE pushbutton switch and observe BUS INDICATOR displays the correct instruction.
- g. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- *h.* Press INITIATE pushbutton switch and verify that the BUS INDICATOR displays the correct instruction.
- 83. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 84. Set the MEMORY guarded switch to the UNPROTECTED position.
- 85. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- 86. Set the ASR toggle switches to 277772.
- 87. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62501776.
- 88. Set the WSR toggle switches to 62500476.
- 89. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 90. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62500476.
- 91. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 92. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 62500476.
- 93. Set the ASR toggle switches to 277774.
- 94. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100107.
- 95. Set the WSR toggle switches to 74100235.
- 96. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 97. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100235.
- 98. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 99. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 74100235.

THE FOLLOWING PROCEDURES ARE USED TO LOAD THE OFF-LINE DIAGNOSTIC LOADER PROGRAM INTO MEMORY

- 100. Load the off-line diagnostic loader tape (SM-D-752126) on the paper tape reader.
- 101. Set the paper tape reader MODE SELECT toggle switch to STRIP and the PWR switch to ON.
- 102. Set the system status panel RESET SELECT TAPE READER toggle switch to ON.

- 103. Press the system status panel RESET pushbutton switch several times and observe that the loader tape moves.
- 104. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 105. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 106. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 107. Set the WSR toggle switches to 00277750.
- 108. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00277750.
- 109. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 110. Set the RUN/ONE INSTR toggle switch to RUN.
- 111. Press the INITIATE pushbutton switch and observe:
 - a. Diagnostic loader tape strip loads into memory.
 - b. PRGM HALT indicator illuminates at the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00277777.
- 112. Rewind the loader tape by setting the system status panel TAPE READ REWIND toggle switch to ON.

THE FOLLOWING PROCEDURES LOAD THE DIAGNOSTIC PROGRAM INTO MEMORY

- 113. Load the Paper Tape Reader/Punch (SM-D-751722) and FACP (SM-D-751719) diagnostic program tapes on the paper tape reader.
- 114. Set the paper tape reader MODE SELECT toggle switch to REEL and the PWR switch to ON.
- 115. Press the NORMAL HALT pushbutton switch and observe that the PRGM HALT indicator extinguishes and the PRCS HALT indicator illuminates.
- 116. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 117. Set the WSR toggle switches to 00000500.
- 118. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00000500.
- 119. Press the system status panel RESET pushbutton switch several times and observe that the diagnostic tape moves.
- 120. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 121. Press the INITIATE pushbutton switch and observe that:
 - a. Diagnostic program tape loads into memory.
 - b. PRGM HALT indicator illuminates at the completion of tape loading.
 - c. BUS INDICATOR displays a reading of 00000631.
- 122. Press the INITIATE pushbutton switch a second time to read-in the 2nd segment of the diagnostic program. Observe that the same indications obtained in step 121 above are obtained.

THE FOLLOWING PROCEDURES ARE USED TO PERFORM THE PROGRAMMED PORTION OF THE PTP AND PTR

- 123. Visually inspect that at least 1/4 reel of tape is loaded on the paper tape punch.
- 124. Set the LINE-OFF-LOCAL rotary switch to LINE.
- 125. Press the paper tape punch ON pushbutton switch.
- 126. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 127. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- 128. Set the ASR toggle switches to 15631.
- 129. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00015631.

- 130. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 131. Set the WSR toggle switches to 22017100.
- 132. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 22017100.
- 133. Set the OPERATIONAL CONTROL rotary switch to STORE SEQL.
- 134. Set the WSR toggle switches to the instruction entries listed in the table below and set the ASR toggle switches to the listed address locations. Press the INITIATE pushbutton switch after each setting and observe the BUS INDICATOR displays the entered data.

Address location		Instruction	
(To allow for writing t 15631	the end of record (377 22017100) before generating th TRU	e trailer) PATCH
17100	5520377	CLAC	/377
17101	0106252	SSS	WTDTPP
17102	0017102	HLT	*
17103	55016435	CLA	CHDLY
17104	26016437	TSA	IDLE
17105	26015554	TSA	PUHDTR
17106	22015632	TRU	RTN
(To initialize the dela	y time to characters/s	econd)	
11252	22011600	TRU	PATCH
11600	55200310	CLAC	/310
11601	60016266	STR	DELTIM
11602	7000000	LXA	0, 1
11603	55200000	CLAC	/0
11604	22011253	TRU	RTN
(To allow for increase	ed timing)		
11463	72000001	IXA	1, 1
11646	22011605	TRU	PATCH
11605	55411610	CLA	TABLE-A, 1
11606	24011471	TRZ	PTDEL
11607	22011465	TRU	RTN
(To allow for testing	the last time through)		
11453	55200001	CLAC	01
11454	12015746	ADD	CHSRED
11455	02200037	LGMC	/37
11456	60015746	SIR	CHSRED
11457	05200024	LGEC	/24
11460	22011633	IRU	PATCH
11633	24011463		PIEDBL
11634	55016266		
11030	22011401		
11401	2401147		PIDEL
11402	22011323	IKU	PTIROL
(To allow for consiste	ent premature termina	tion)	DATON
11500	2401/10/	IRZ	PATCH
1/10/	55037774	CLA	WSR
17110	02202000	LGMC	/2000
1/111	24015322		PT12B
1/112	22015631		
111//	24011636		PAICH
11030	00007774		VVOR /2000
11637	02202000		/2000 DT06P
116/1	24010407 22011201		
11041	02202000		F1002D
11440	02202000		12000
(To reduce the size of	of trailer 1 leader)		

15736 00000200

Address location

Instruction

(To allow for reset timing)

11473	7000000
(Delay times)	
11610	00000310
11611	00000303
11612	00000257
11613	00000252
00614	00000233
11615	00000226
11616	00000202
11617	00000175
11620	00000151
11621	00000144
11622	00000120
11623	00000113
11624	00000067
11625	00000062
11626	00000036
11630	00000017
11631	00000005
11632	0000000

- 135. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 136. Set the WSR toggle switches to 00015000.
- 137. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays a reading of 00015000.
- 138. Set the RUN/ONE INSTR toggle switch to RUN.
- 139. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 140. Press the INITIATE pushbutton switch and observe that:
 - a. PRGM HALT indicator illuminates.
 - b. PTP TEST message i generated on page printer.
 - c. BUS INDICATOR displays a reading of 00015014.
- 141. Set the WSR toggle switch bits 00 through 06 to zero.
- 142. Press the INITIATE pushbutton switch and observe that the PRGM HALT indicator illuminates and the BUS INDICATOR displays a reading of 00015310.

THE FOLLOWING PROCEDURES ARE USED TO GENERATE AN ASCII TAPE

- 143. Set the WSR toggle switches to 00000400.
- 144. Press the INITIATE pushbutton switch and observe that:
 - a. ASCII characters are being punched.
 - b. ASCII characters being punched are also generated on the local page printer.
 - c. END OF PT message generated on page printer at the end of 10 blocks of data.
 - d. PRGM HALT indicator illuminates.
 - e. BUS INDICATOR displays a reading of 00015660.

NOTE

To prematurely terminate before 10 lines. of characters are punched, set WSR toggle switch bit 13 to a 1.

145. Press the INITIATE pushbutton on switch and observe that the BUS INDICATOR displays a reading of 00015310.

THE FOLLOWING PROCEDURES ARE USED TO GENERATE THE CONSTANT CHARACTER TAPE REQUIRED FOR THE PTR TIMING TEST

- 146. Set the WSR toggle switches to 00000155.
- 147. Press the INITIATE pushbutton switch and observe that the paper tape punch begins to generate a 155 character tape.
- 148. After approximately 5-feet of data is generated, set WSR toggle switch bit 13 to a 1 and observe that:
 - a. PRGM HALT indicator illuminates.
 - b. BUS INDICATOR displays a reading of 00015660.
 - c. END OF PT message is generated on the page printer.
- 149. Press the NORMAL HALT pushbutton switch and then, in turn, the INITIATE pushbutton switch observe that: *a.* PRGM HALT indicator illuminates.
 - b. BUS INDICATOR displays a reading of 00010014.
 - c. PR TEST message i generated on the page printer.

THE FOLLOWING PROCEDURES EXECUTE THE PAPER TAPE READER TEST

- 150. Set the WSR toggle switches to 00000400.
- 151. Load the ASCII test tape (step 144 above) on the paper tape reader.
- 152. Set the paper tape reader MODE SELECT toggle switch to STRIP and the PWR switch to ON.
- 153. Set the system status panel RESET SELECT TAPE READER toggle switch to ON.
- 154. Press the system status panel RESET pushbutton switch and observe that the ASCII test tape moves.
- 155. Press the INITIATE pushbutton switch and observe that the PRGM HALT indicator illuminates and the BUS
- INDICATOR displays a reading of 00010373. (This indicates that PT-O1 through PT-05 tests have been executed). 156. Press the INITIATE pushbutton switch and observe that:
 - a. Program starts to read the test tape.
 - b. All correct ASCII characters read am generated on the page printer.
 - c. PRGM HALT indicator illuminates at completion of read-in.
 - d. BUS INDICATOR displays a reading of 00011232.
 - e. END OF PTS-SYNC TEST message is generated on the page printer.

NOTE

If the ASCII test tape was generated with less than 10 blocks of data (step 144 above), the reading of the tape must be terminated (WSR bit 13 to a 1) at the start of the last block of data.

157. If the program does not halt at the completion of the tape read-in, press the NORMAL HALT pushbutton switch and observe what numerical range the BUS INDICATOR is displaying:

Range

Remarks

10576 to 10745

- If no ASCII characters are printed on the local page printer, the program never found the beginning of record which is a 377 character.
 - If the ASCII characters are printed on the local page printer, the program never found the end of record which is a 377 character.
- 158. At this point in the diagnostic program, three options are available to the reader. It is recommended however, that option 1 be used:

Option 1 - PTR Timing Test

- a. Press the INITIATE pushbutton switch and observe that:
 - (1) PRGM HALT indicator illuminates.
 - (2) BUS INDICATOR displays a reading of 00011274.
 - (3) SET WSR to CHAR message is generated on the page printer.
- b. Proceed to step 159 below.

Option 2 - Rerun PTR Test

- *a.* Press the NORMAL HALT pushbutton switch and then, in turn, the INITIATE pushbutton switch and observe that:
 - (1) PRGM HALT Indicator illuminates.
 - (2) BUS INDICATOR displays a reading of 00011233.
- b. Press the INITIATE pushbutton switch a 2nd time and observe that:
 - (1) PRGM HALT Indicator illuminates.
 - (2) BUS INDICATOR displays a reading of 00010373.
- c. Proceed to step 150 above.

Option 3 - Run PTP Test

- a. Press the NORMAL HALT pushbutton switch and, in turn, the INITIATE pushbutton switch and observe that:
 (1) PRGM HALT Indicator illuminates.
 - (2) BUS INDICATOR displays a reading of 00011233.
- b. Press the NORMAL HALT and INITIATE pushbutton switch a 2nd time and observe that:
 (1) PRGM HALT indicator illuminates.
 - (2) BUS INDICATOR displays a reading of 00015014.
- c. Proceed to step 143 or 146 above.

THE FOLLOWING PROCEDURES EXECUTE THE PTR TIMING TEST

- 159. Load the constant character test tape (step 148 above) on the paper tape reader.
- 160. Set the paper tape reader MODE SELECT toggle switch to STRIP and the PWR switch to ON.
- 161. Set the system status panel RESET SELECT TAPE READER toggle swish to ON.
- 162. Press the system status panel RESET pushbutton switch several times and observe that the test tape moves.
- 163. Set the WSR toggle switches to 00000155.
- 164. Press the INITIATE pushbutton switch and observe that the PRGM HALT Indicator illuminates and the BUS INDICATOR displays a reading of 00011300.
- 165. At this point in the diagnostic program, two options are available to the reader. It is recommended, however, that option 1 be used:

Option 1 - Automatic PTR Timing Test

- *a.* Press the NORMAL HALT and then the INITIATE pushbutton switches and observe that the tape is reading 10 characters per block and each block at a different rate, starting at 5 characters per second and increasing in increments to 200 characters per second.
- b. After approximately 3 minutes, set WSR toggle swish bit 13 to a 1 and observe that:
 - (1) PRGM HALT Indicator illuminates.
 - (2) BUS INDICATOR displays a reading of 00011232.
- **Option 2 Manual PTR Timing Test**
 - a. Press the INITIATE pushbutton switch and observe that the PRGM HALT Indicator illuminates and the BUS INDICATOR displays a reading of 00011315.
 - b. Select a delay time for the characters per second desired from the chart below and enter it in WSR toggle switch bits 16 through 23.

Characters per second	Time Delay (ms)	WORK SWITCH REGISTER bit 16-23
5	200	310
10	195	303
30	175	257
35	170	252
50	155	233
55	150	226
75	130	202
80	125	175
100	105	151
105	100	144
125	80	120
130	75	113
150	55	067
166	50	062
175	30	036
180	65	031
190	15	017
200	5	005

NOTE

WSR toggle switch bits 16 through 23 permit time delay selections from zero through 255. However, character frequencies less than 5/seconds or greater than 200/seconds cannot be selected.

- c. Press the INITIATE pushbutton switch and observe that the tape is read-in at the rate specified in *b* above.
- d. After approximately 3-minutes, set WSR toggle switch bit 15 to a 1 and observe that:
 - (1) PRGM HALT indicator illuminates.
 - (2) BUS INDICATOR displays a reading of 00011232.

Section III. POSSIBLE PROGRAM HALTS

Halt address

Remarks

10422	WSR toggle switches incorrectly set.
11016 or 11111	CHRDY is not getting set. Press the system status
	panel RESET pushbutton switch and then the
	INITIATE pushbutton switch to continue.
10735	1200 characters were read without detecting the first character.

BIT POSITION	17	18	19	20	21		22	23	24
	•	•	Ð	•	•	٠	0	0	0
SOM						٠			0
EOA								0	
EOM						٠		0	0
EOT						٠	•		
WRU						٠	•		۲
RU						•	•	0	
BELL						•	0	٠	٠
FE					•	٠			
H. TAB					•	•			٠
LINE FEED					•	•		۲	
VT					•	٠		٠	•
FORM					•	٠	0		
RETURN					0	•	٠		•
SO					•		٠	٠	
SL					•	•	•	٠	٠
DC				•		•			
X-ON				•					•
TAPE AUX ON				•		•		٠	
				•		•		0	•
TAPE AUX OFF				•		٠	•		
ERROR				•			6		
SYNC				•		•	•	•	
LEM				•		•	•	•	0
S				•	•	•			
S ₁				6	0				•
S ⁺				•		•		•	
S				0	•	•		•	0
S ₁				0	•	•	0		
ST				•	•	•	٠		•
S				•	•		•		
S7				ò	•		0	•	0
NULL						٠			

BIT POSITION	17 1	8 19	20	21		22	23	24
	• •	•		•	•	•	•	0
1		•						•
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#		•					•	۵
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r. R.					•			•
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•					•		•	•
3					•			
-					• ,		•	•
•				•	٠			•
			•	•	•		•	•
U 7			•		•			-
		•			•		-	•
2			0		٠		•	-
3					•	÷	0	9
4		•	•		٠			
5		•	•		٠	•		•
0		•	•		٠	۲	٠	
7		•	0		٠	•	•	•
8		•	Ø	•	٠			
9		•	•	0	٠			•
:		•	•	٠	٠		٠	
5		•	•	0	٠		•	•
<		•	0	•	٠	•		
		•	0	0	٠	•		٠
>		٠	٠	•	٠	۲	•	
?		•	•	•	٠	•	۲	•
••								

BIT POSITION	17	18	19	20	21		22	23	24
	•	•	•	•	0	•	•	0	0
A		•							•
В		•				• .		•	
C		•				•		9	0
D		0				•	٠		
E		•				•	•		0
F		•				•	•		
G		0				٠	•	٠	0
H		•			•	•			
I		•			0	•			•
J		9			0	•		9	
K		•			9	٠		•	
مل		0			•	•	•		
M		•			9	•	•		•
N		6			•	٠	•	•	
0		9			0	٠	٠	•	0
P		•		•		•			
Q		•		•		•			•
a		•		•		•		•	
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1		•		0		•	۲		
U V		•		•		•	•		0
4 W		•		0		•	•	•	
T I		-		•		٠	•	0	0
T T		•		•	0	•			
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BIT	POSITION	17	18	19	20	21		22	23	24
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			•	Q			٠		•	•
			•	•					6	U
			•	Ð			٠	•		
			0	9			٠	•		•
			•	0			٠	0	٠	
			0	0			•	0	٠	ø
			•	•		•	•			
			•			0	٠			•
			•	Ø		9	٠		0	
			•	0		0	•		0	•
			0	•		0	٠	0		
			•	0.0		0	٠	•		•
			•	0		0	٠	٠	0	
			•	9		0	٠	٠	•	•
			9	0	•		•			
			•	•	0		٠			•
			•	•	0				•	
			•	•	•		•		0	0
			•	•	0		٠	۲		
			0	0	0		•	•		•
			•	۲	•		•	•	0	
			•	•	•		•	•	•	•
			•	•	0	0	•			
			•	0	8	0	٠			•
			0	•	0	0	•		•	
			•	•	0	0	•		•	0
AC	K		•	•	•	•	•	•		
AL	T MODE		0	•	•	0	•	•		•
ES(C		•	•	0	Ø	•	•	•	
RU	B OUT		•	0	0	0	•	•	0	0

Section V. MAINTENANCE ERROR PRINTOUTS

	Printout		Probable cause		Corrective action
While ru of t bef	unning PRT/PTP off-line test, any he following printouts may occur ore END OF PT printout:				
a.	Set WSR to CHAR.	a.	WORD SWITCH REGISTER not set properly for PTR timing test.	а.	Set tape format code in WORD SWITCH REGISTER bits 14-23 and press INITIATE
b.	PT <u>XX</u> -01 where <u>XX</u> is 01, 02 or 03.	b.	Status register failed.	b.	Replace following PTR synchronizer cards in sequence. Repeat test after each replacement. (1) MOS2 (2) MOS3
С.	PT <u>XX</u> -02 where <u>XX</u> is 01, 02 or 03.	с.	PTR not ready.	C.	 Check reader for tape and position of LOOP/REEL switch. (1) Replace PTR synchronizer MOS2 card. Repeat test. (2) Replace PTR. Repeat test.
d.	PT <u>XX</u> -03 where <u>XX</u> is 02 or 04.	d.	Status register failed.	d.	Replace following PTR synchronizer cards in sequence. Repeat test after each replacement. (1) MOS2 (2) MOS3
e.	PT <u>XX</u> -01 where <u>XX</u> is 04 or 05.	e.	PTR not ready.	e.	 Check reader for tape and position of LOOP/REEL switch. (1) Replace PTR synchronizer MOS2 card. Repeat test. (2) Replace PTR. Repeat test.
f.	PT 04-02.	f.	Buffer register failed to clear.	f.	Replace following PTR cards in sequence. Repeat test after each replacement. (1) MOS3 (2) MOS2 (3) MOS1
g.	PT04-04.	g.	PTR not ready.	g.	 (c) MOOT Check reader for tape and position of LOOP/REEL switch. (1) Replace PTR synchronizer MOS2 card. Repeat test. (2) Replace PTR. Repeat test.
h.	PT05-02.	h.	Status register failed.	h.	Replace following PTR synchronizer in sequence. Repeat test after each replacement. (1) MOS2 (2) MOS3
i.	PT05- <u>XX</u> where <u>XX</u> is 03, 04, 05 or 06.	i.	Data read from PTR synchronizer buffer differs from data written into it by test program. Data written was as follows: $\underline{XX} = 03$ data was 377 $\underline{XX} = 04$ data was 252 $\underline{XX} = 05$ data was 125 $\overline{XX} = 06$ data was 000	i.	 Replace following PTR synchronizer cards in sequence. Repeat test after each replacement. (1) MOS3 (2) MOS2 (3) MOS1
j.	PT06- <u>XX</u> where <u>XX</u> is 01 or 10.	j.	CH RDY set too fast.	j.	Replace following PTR synchronizer cards in sequence. Repeat after each replacement. (1) MOS3 (2) MOS2
k.	TE PRT TOOK <u>AAA</u> for CH RDY to SET. PT06- <u>XX</u> where <u>XX</u> is 02, 09 or 77, and <u>AAAA</u> is actual time between characters received.	k.	CH RDY failed to set within allotted time.	k.	Replace following in sequence. Repeat test after each replacement. (1) Receiver cards (2) PTR synchronizer MOS 3 card.

	Printout		Probable cause		Corrective action
I.	PTG06- <u>XX</u> where <u>XX</u> is 05 or 12.	I.	Status register failed.	I.	 (3) PTR synchronizer MOS2 card. (4) Paper tape reader. Replace following PTR synchronizer cards in sequence. Repeat test after each replacement. (1) MOS2 (2) MOS3
m.	PT06-07	m.	No start character received. (1) Data buffer (2) PTR error	m.	 Check tape to be sure start character (377) is present and passed under read head. (1) Replace PTR synchronizer MOS3 card. Repeat test. (2) Replace PTR. Repeat test
n.	PTR READ ERROR DATA XXX DATA EXPECTED YYY DELAY ZZZMS PT06-14 where XXX is format code for character read and YYY is format code for character expected. ZZZ is actual delay between characters received. Find XXX and YYY for ASCII codes.	n.	Format selection, data input or PTR. (1) Data input	n.	 (c) Hopker PTR Hopker Kok (c) Hopker First Hopker Kok (d) Replace following PTR cards in sequence. Repeat test after each replacement. (a) Receivers (b) MOS3 (c) MOS1
0.	PT <u>XX</u> -01 where <u>XX</u> is 07, 10, 11, 12, 13.	0.	Status register failed.	0.	 (2) Replace FTR. Repeat test. Replace following PTR synchronizer cards in sequence. (1) MOS2 (2) MOS3
р.	PT08-02	р.	Status register failed.	р.	Replace following PTP synchronizer cards in sequence. Repeat test after each replacement. (1) MOS2 (2) MOS3
q.	PT10-02	q.	Buffer register failed to clear.	q.	Replace following PTP synchronizer cards in sequence. Repeat test after each replacement. (1) MOS3 (2) MOS2 (3) MOS1
r.	PT10-03	r.	Status register failed.	r.	Replace following PTP synchronizer cards in sequence. Repeat test after each replacement. (1) MOS2 (2) MOS3
S.	PT11- <u>XX</u> where <u>XX</u> is 02, 03. 04 or 05.	S.	Data read from PTP synchronizer buffer differs from data written into it by test program. Data written was as follows: XX = 02 data was 377 XX = 03 data was 262 XX = 04 data was 125 XX = 05 data was 000	S.	 Replace following PTP synchronizer cards in sequence. Repeat test after each replacement. (1) MOS3 (2) MOS2 (3) MOS1
t.	PT12- <u>XX</u> where <u>XX</u> is 01 or 02.	t.	Timing error.	t.	Replace following PTP synchronizer cards in sequence. Repeat test after each replacement. (1) MOS3

(2) MOS2

	Printout		Probable cause		Corrective action
u.	PT13-01	u.	PTR not ready.	u.	Check reader for tape and position of LOOP/REEL switch. (1) Replace PTR synchronizer MOS2 card_Repeat test
V.	PT13- <u>XX</u> where <u>XX</u> is 02 or 10.	V.	CH RDY set too fast.	V.	 (2) Replace PTR. Repeat test. Replace following PTR synchronizer cards in sequence. Repeat test after each replacement. (1) MOS3
W.	PTR READ ERROR DATA XXX DATA EXPECTED YYY DELAY ZZZ MS PT13-03 where XXX is format code for character expected, ZZZ is actual delay between characters received. Find XXX and YYY for ASCII characters.	w.	Format selection, data input or PTR. (1) Data input.	W.	 (2) MOS2 Check that format selection (WSR 14-23) is correct for tape being read. (1) Replace following PTR cards in sequence. Repeat test after each replacement. (a) Receivers (b) MOS3 (c) MOS1 (2) Replace PTR. Repeat test.



Figure 3 (1). Paper tape reader logic data flow diagram (Sheet 1 of 7).



Figure 3 (2). Paper tape reader logic data flow diagram (Sheet 2 of 7).



Figure 3 (3). Paper tape reader logic data flow diagram (Sheet 3 of 7).



Figure 3 (4). Paper tape reader logic data flow diagram (Sheet 4 of 7).


Figure 3 (5). Paper tape reader logic data flow diagram (Sheet 5 of 7).



Figure 3 (6). Paper tape reader logic data flow diagram (Sheet 6 of 7).



Figure 3 (7). Paper tape reader logic data flow diagram (Sheet 7 of 7).



Figure 4 (1). Paper tape reader timing test logic data flow diagram (Sheet 1 of 4).



Figure 4 (2). Paper tape reader timing test logic data flow diagram (Sheet 2 of 4).



Figure 4 (3). Paper tape reader timing test logic data flow diagram (Sheet 3 of 4).



Figure 4 (4). Paper tape reader timing test logic data diagram (Sheet 4 of 4).



Figure 5 (1), Paper tape punch logic data flow diagram (Sheet 1 of 3).



Figure 5 (2). Paper tape punch logic data flow diagram (Sheet 2 of 3).



Figure 5 (3). Paper tape punch logic data flow diagram (Sheet 3 of 3).

EXHIBIT J

RESTORING OPERATIONAL PROGRAM

Section I. GENERAL

The diagnostic programs are essentially divided into two groups. If either the Maintenance Control Panel, Central Processor, Memory, Bootstrap, or Memory-to-Memory diagnostic programs are executed, the procedures outlined in Section II must be performed in order to restore the AN/TTC-38(V) to an operating condition. If the Common Control Synchronizer, Remote Device, Functional Assignment Control Pane, or Paper Tape Reader/Paper Tape Punch diagnostic programs are executed, the procedures outlined in Section III must be performed in order to restore the equipment to an operating condition.

Section II. INITIAL SETUP OF EQUIPMENT

- 1. Set all WSR toggle switches to 0 (down).
- 2. Set CLOCK OPERATE CONTROL rotary switch to CONT.
- 3. Set MEMORY guarded switch to UNPROTECTED position.
- 4. Set REGISTER SELECT rotary switch to MEM and the OPERATIONAL CONTROL to STORE SEQLY.
- 5. Set RUN/ONE INSTR toggle switch to RUN.
- 6. Press COORDINATE and INITIATE pushbutton switches and observe that ACTIVE Indicator lights.
- 7. Press NORMAL HALT pushbutton switch twice and observe that PRCS HALT indicator lights.
- 8. Set OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 9. Set RUN/ONE INSTR toggle switch to ONE INSTR.
- 10. Press CLEAR pushbutton.
- 11. Set WSR toggle switches to 00277750.
- 12. Press INITIATE pushbutton switch and observe that BUS INDICATOR display reads 00277750.
- 13. Set OPERATIONAL CONTROL rotary switch to STORE SEQLY and the REGISTER SELECT to MEM.
- 14. Set WSR toggle switches to the instruction entries listed in attached chart and press INITIATE pushbutton after each setting. Observe that BUS INDICATOR displays entered instruction.

Address	Instruction
00277750	01077751
00277751	00002404
00277752	05200377
00277753	24077755
00277754	22077750
00277755	70100000
00277756	7000001
00277757	01077760
00277760	00002400
00277761	02200040
00277762	24077757
00277763	01077764
00277764	00002404
00277765	34000020

Address	Instruction
00277766	35000010
00277767	72000001
00277770	7400003
00277771	22077757
00277772	62501776
00277773	72100001
00277774	74100107
00277775	22077756
00277776	0000000

- 15. Press NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator lights.
- 16. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 17. Set the WSR toggle switches to 00277750.
- 18. Press the INITIATE pushbutton switch and observe that BUS INDICATOR displays 00277750.
- 19. Set the OPERATIONAL CONTROL rotary switch to CONT PNL INSTR and the REGISTER SELECT to position A.
- 20. Set the WSR toggle switches to 55137754.
- 21. Press INITIATE pushbutton switch and observe that the BUS INDICATOR reading agrees with the entries specified on the chart.

NOTE

The following procedures will correct an erroneous address entered from the chart of specified addresses and instructions.

- a. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- b. Set the ASR toggle switches to the correct address.
- c. Press INITIATE pushbutton switch and observe that the BUS INDICATOR displays the correct address.
- *d.* Set the WSR toggle switches to the *correct instruction number*.
- e. Set the OPERATIONAL CONTROL rotary switch to STORE.
- f. Press INITIATE pushbutton switch and observe BUS INDICATOR displays the correct instruction.
- g. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- *h.* Press INITIATE pushbutton switch and verify that the BUS INDICATOR displays the correct instruction.
- 22. Place operational program strip tape (SM-D-751709 on paper tape reader.
- 23. Set paper tape reader MODE SELECT toggle switch to STRIP and POWER ON/OFF toggle switch to ON.
- 24. Set system status panel RESET SELECT TAPE READER toggle switch to ON.
- 25. Press system status panel RESET pushbutton switch several times and observe that tape strip moves.
- 26. Press NORMAL HALT pushbutton switch and observe that PRCS HALT indicator lights.
- 27. Set OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 28. Set RUN/ONE INSTR toggle switch to ONE INSTR.
- 29. Set WSR toggle switches to 00277750.
- 30. Press INITIATE pushbutton switch and observe that BUS INDICATOR displays 00277750.
- 31. Set OPERATIONAL CONTROL rotary switch to CMPT.
- 32. Set RUN/ONE INSTR toggle switch to RUN.

- 33. Press INITIATE pushbutton switch and observe:
 - a. Tape begins to load into memory.
 - b. PRGM HALT indicator lights at end of tape loading.
 - c. BUS INDICATOR displays 00277777 at completion of tape read-in.
- 34. Remove operational program tape strip.
- 35. Press NORMAL HALT pushbutton switch and observe PRCS HALT Indicator lights.
- 36. Set OPERATIONAL CONTROL rotary switch to STORE and REGISTER SELECT to PEX.
- 37. Set WSR toggle switches to 00002000.
- 38. Press the CLEAR and INITIATE pushbutton switches, in turn, and observe BUS INDICATOR displays 00002000.
- 39. Place page 0, 1, and 2, each in turn, on paper tape reader and press the system status panel RESET pushbutton switch several times and observe that the tape(s) move.
- 40. Set OPERATIONAL CONTROL rotary switch to CMPT.
- 41. Set RUN/ONE INSTR toggle switch to RUN.
- 42. Press INITIATE pushbutton switch and observe tapes start to load and when complete BUS INDICATOR displays 00002056 and the PRGM HALT indicator lights.
- 43. Set system status panel TAPE REWIND switch to ON and remove the data base tapes when rewound.
- 44. Place current directory tape on paper tape reader and press system status RESET pushbutton switch several times to see if tape moves.
- 45. Press NORMAL HALT pushbutton switch and observe PRCS HALT indicator lights.
- 46. Set MEMORY guarded switch to PROTECTED position.
- 47. Check to be sure the REAL TIME CLOCK rotary switch is set to the ENABLE position.
- 48. Set OPERATIONAL CONTROL rotary switch to STORE and REGISTER SELECT to PEX.
- 49. Set WSR toggle switches to 00240000 for the AN/TTC/38(V)1 or to 60240000 for the AN/TTC-38(V)2.
- 50. Press INITIATE pushbutton switch and observe BUS INDICATOR displays either 00240000 or 60240000.
- 51. Set OPERATIONAL CONTROL rotary switch to CMPT.
- 52. Press INITIATE pushbutton switch and observe that the ACTIVE Indicator is illuminated.
- 53. Set function code to 13.
- 54. Set ASR bit 21 to a 1 to read in current directory tape.
- 55. Press READ pushbutton switch.
- 56. Rewind the current directory after completion.
- 57. Load the patch tapes, if any, in the paper tape reader.
- 58. Set MEMORY guarded switch to UNPROTECTED position.
- 59. Set ASR bit 22 to 1 read in the patch tapes.
- 60. Press READ pushbutton switch for each patch tape.
- 61. At the completion, set the MEMORY guarded switch to the PROTECTED position.
- 62. Load the data base update tape(s), if required, on the paper tape reader.
- 63. Set ASR bit 23 to a 1 to read the data base update tape(s).
- 64. Press the READ pushbutton switch for each data base update tape.
- 65. If the PROCESSOR STATUS ON-LINE indicator illuminates, set the function code to 03.
- 66. Press READ pushbutton switch.

Section III. RESTORING PRELOADER

- 1. Press NORMAL HALT pushbutton switch and observe that PRCS HALT indicator illuminates.
- 2. Set RUN/ONE INSTR toggle switch to ONE INSTR.
- 3. Set the ASR toggle switches to 00277772.
- 4. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY and the REGISTER SELECT to MEM.
- 5. Press the INITIATE pushbutton switch and observe that BUS INDICATOR displays a reading of 62500476.
- 6. Set the MEMORY guarded switch to the UNPROTECTED position.
- 7. Set the WSR toggle switches to 62501776.
- 8. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 9. Press the INITIATE pushbutton switch and observe that BUS INDICATOR displays a reading of 62501776.
- 10. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 11. Press the INITIATE pushbutton switch and observe that BUS INDICATOR displays a reading of 62501776.
- 12. Set the ASR toggle switches to 277774.
- 13. Press the INITIATE pushbutton switch and observe that BUS INDICATOR displays a reading of 74100235.
- 14. Set the WSR toggle switches to 74100107.
- 15. Set the OPERATIONAL CONTROL rotary switch to STORE.
- 16. Press the INITIATE pushbutton switch and observe that BUS INDICATOR displays a reading of 74100107.
- 17. Set the OPERATIONAL CONTROL rotary switch to MEMORY DISPLAY.
- 18. Press the INITIATE pushbutton switch and observe that BUS INDICATOR displays a reading of 74100107.
- 19. Set all WSR toggle switches to 0's.
- 20. Set the CLOCK OPERATE CONTROL rotary switch to CONT.
- 21. Set the MEMORY guarded switch to the PROTECTED position.
- 22. Set the REGISTER SELECT rotary switch to MEM and the OPERATIONAL CONTROL to STORE SEQL.
- 23. Set the RUN/ONE INSTR toggle switch to RUN.
- 24. Press the COORDINATE and INITIATE pushbutton switches and observe that the ACTIVE Indicator illuminates.
- 25. Place the operational program strip tape (SM-D-751709) on the paper tape reader.
- 26. Set the paper tape reader MODE SELECT toggle switch to STRIP and the POWER ON/OFF to ON.
- 27. Set the system status panel RESET SELECT TAPE READER toggle switch to ON.
- 28. Press the system status pane RESET pushbutton switch several times and observe that the operational program strip tape moves.
- 29. Press the normal HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 30. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 31. Set the RUN/ONE INSTR toggle switch to ONE INSTR.
- 32. Set the WSR toggle switches to 00277750.
- 33. Press the INITIATE pushbutton switch and observe that the BUS INDICATOR displays 00277750.
- 34. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 35. Set the RUN/ONE INSTR toggle switch to RUN.

- 36. Press the INITIATE pushbutton switch and observe that:
 - a. Operational program strip tape loads into memory.
 - b. PRGM HALT indicator illuminates at end of loading process.
 - c. BUS INDICATOR displays 00277777.
- 37. Remove the tape strip from the paper tape reader.
- 38. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator illuminates.
- 39. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 40. Set the WSR toggle switches to 00002000.
- 41. Press the INITIATE and CLEAR pushbutton switches, in turn, and observe that the BUS INDICATOR displays 00002000.
- 42. Place page 0 on the paper tape reader.
- 43. Set the paper tape reader MODE SELECT toggle switch to READ and press the system status panel RESET pushbutton switch several times and observe that the data base tape moves.
- 44. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 45. Set the RUN/ONE INSTR toggle switch to RUN.
- 46. Press the INITIATE pushbutton switch and observe that:
 - a. Data base tape (page 0) loads into memory.
 - b. PRGM HALT indicator illuminates at end of loading process.
 - c. BUS INDICATOR displays 00002056.
- 47. Set the system status panel TAPE REWIND toggle switch to ON and then remove the tape reel from the paper tape reader.
- 48. Press the NORMAL HALT pushbutton switch and observe that the PRCS HALT indicator Illuminates.
- 49. Set the REAL TIME CLOCK toggle switch to ENABLE.
- 50. Set the OPERATIONAL CONTROL rotary switch to STORE and the REGISTER SELECT to PEX.
- 51. Set the WSR toggle switches to 00240000 for the AN/TTC-38(V)1 or to 60240001 for the AN/TTC-38(V)2.
- 52. Press the INITIATE pushbutton switch and observe the BUS INDICATOR displays 00240000 or 60240001.
- 53. Set the OPERATIONAL CONTROL rotary switch to CMPT.
- 54. Press the INITIATE pushbutton switch and observe that the ACTIVE indicator illuminates.
- 55. Place the current directory tape reel on the paper tape reader.
- 56. Set the paper tape reader MODE SELECT toggle switch to REEL and the POWER ON/OFF to ON.
- 57. Press the system status panel RESET pushbutton switch several times and observe that the tape reel move.
- 58. Set the function code to 13.
- 59. Set ASR bit 21 to a 1 and press the READ pushbutton switch to read in the current directory.
- 60. Rewind the current directory after completion.
- 61. Load the data base update tapes, If required, in the paper tape reader.
- 62. Set the MODE SELECT switch to STRIP.
- 63. Set ASR bit 23 to a 1 and press the READ pushbutton to read in the data base update tapes
- 64. If the PROCESSOR STATUS ON-LINE indicator illuminates, set the function code to 03 and press the READ pushbutton switch to connect the processor to the network.

By Order of the Secretary of the Army:

Official:

BERNARD W. ROGERS General, United States Army Chief of Staff

PAUL T. SMITH Major General, United States Army The Adjutant General

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ARNG & USAR: None. For explanation of abbreviations used, see AR 310-50.